Group 7 Semiconductor Research Capstone Requirements

1. **Geometric requirements**
    1. Top electrode thickness must be greater than 100nm but less than 200nm.
        1. Verify thickness with scanning electron microscope.
    2. Bottom electrode thickness must be greater than 100nm but less than 200nm.
        1. Verify thickness with scanning electron microscope.
        2. Active Layer must be fabricated at different thicknesses.
            1. 10nm
            2. 20nm
            3. 100nm
    3. Patterning must be done with shadow mask for various feature sizes.
        1. 100um
        2. 50um
        3. 25um
        4. 10um
2. **Material Requirements**
    1. Top electrode must be nickel.
    2. Active layer must be WO3.
    3. Bottom electrode must be nickel.
    4. All material properties may be verified with Energy Dispersive Spectroscopy- line scan.
3. **Fabrication Requirements**
    1. Vacuum Pressure must be below 9.99 *10^-6 Torr when doing vapor deposition.
    2. Deposition rate must be recorded.
4. **Testing Requirements**
    1. Multiple devices must be tested.
        1. Different feature Sizes
            1. 100um feature size
                1. 10nm thickness
                2. 20nm thickness
                3. 100nm thickness
            2. 50um feature size
                1. 10nm thickness
                2. 20nm thickness
                3. 100nm thickness
            3. 25um feature size
                1. 10nm thickness
                2. 20nm thickness
                3. 100nm thickness
    2. For each feature size and thickness 10 devices must be tested, and data must be compared to evaluate Device to Device (D2D) variation.
    3. For each feature size and thickness 20 switching cycles must be performed to evaluate cycle to cycle (C2C) variation.
    4. Memory Performance Testing

1. I-V curves
    1. Non-linearity
    2. Memory Window
    3. Set and Reset voltages
    4. 20 cycles to find variation in Set and Reset voltages
        1. Use statistical methods to find the mean, median, mode, first and third quartile.
2. Multi-level cell (MLC) demonstration
    1. DC MLC testing
        1. Vary the compliance current
        2. Vary the reset stop voltage
    2. AC MLC testing
        1. Modulate pulse width and height.
        2. Make contour plot with pulse width vs pulse height with colored contours for resistance.
    3. D2D variation testing of MLC states or LRS/HRS
        1. Plot of probability density versus resistance for each MLC state.
            1. For each feature size
                1. For each thickness for each feature size.
    4. C2C variation testing of MLC states or LRS/HRS
        1. Plot of probability density versus resistance for each MLC state.
            1. For each feature size.
                1. For each thickness for each feature size.
                2.
3. Retention characteristics extrapolated to 10^12 seconds or as long as possible.
4. Endurance testing must be done for 10^9 switching cycles.

5. **Characterization Requirements**

1. Modelling must be done to characterize different regions of the I-V data
    1. Mathematical current conduction model.
        1. Evaluate all known types of dielectric conduction and compare to I-V data to figure out dominant mechanisms.
            1. Create plots of electric field, voltage, and temperature versus current density to evaluate predict mechanisms.
            2. **If it is proving difficult to create a model, further temperature testing must be done.**
            3. Extraction of the barrier height must be **ATTEMPTED**.
    2. Use the Dr. Chen method to extract activation energy.
2. Qualitative characterization of the switching mechanism must be **ATTEMPTED.**
    1. Examine feature size effects.
    2. Examine thickness effects.
3. Simulation will only be required if the current conduction mechanism has been characterized.
    1. Collaborate with SDRL researcher Kaitlyn to plot temperature.