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Tungsten Oxide-based Resistive Memory

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Abstract

Among the various emerging memories, resistive random-access memory (RRAM) has attracted much attention owing to the ultrahigh scalability, non-destructive sensing, simple structure, and low power consumption. The purpose of this project is to develop an emerging memory device which enable storage and high operation speed for the demands of current computing applications in the area of microelectronics. A Tungsten Oxide (WO_x)-based RRAM with Indium Tin Oxide (ITO) electrodes is presented in this work. The WOx active layer thickness was the key analysis parameter. Moreover, its endurance and retention abilities are investigated as well as device-to-device variation. In addition, UV-visible spectroscopy was utilized to study the optical properties of WO_x-based RRAMs.

Approach

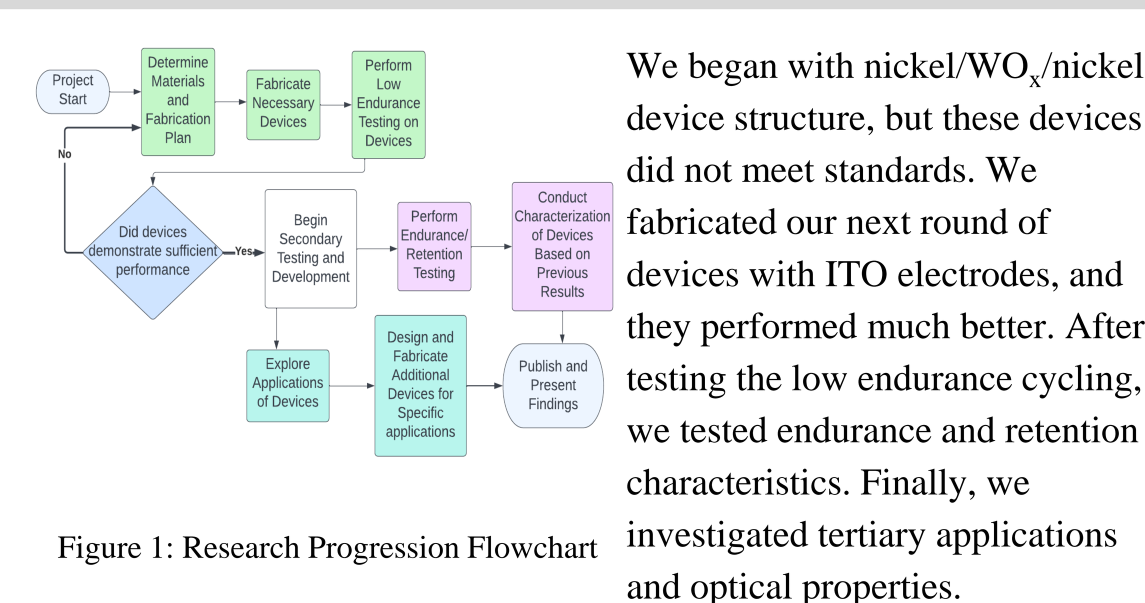

Figure 1: Research Progression Flowchart

We began with nickel/WO_x/nickel device structure, but these devices did not meet standards. We fabricated our next round of devices with ITO electrodes, and they performed much better. After testing the low endurance cycling, we tested endurance and retention characteristics. Finally, we investigated tertiary applications and optical properties.

Methods

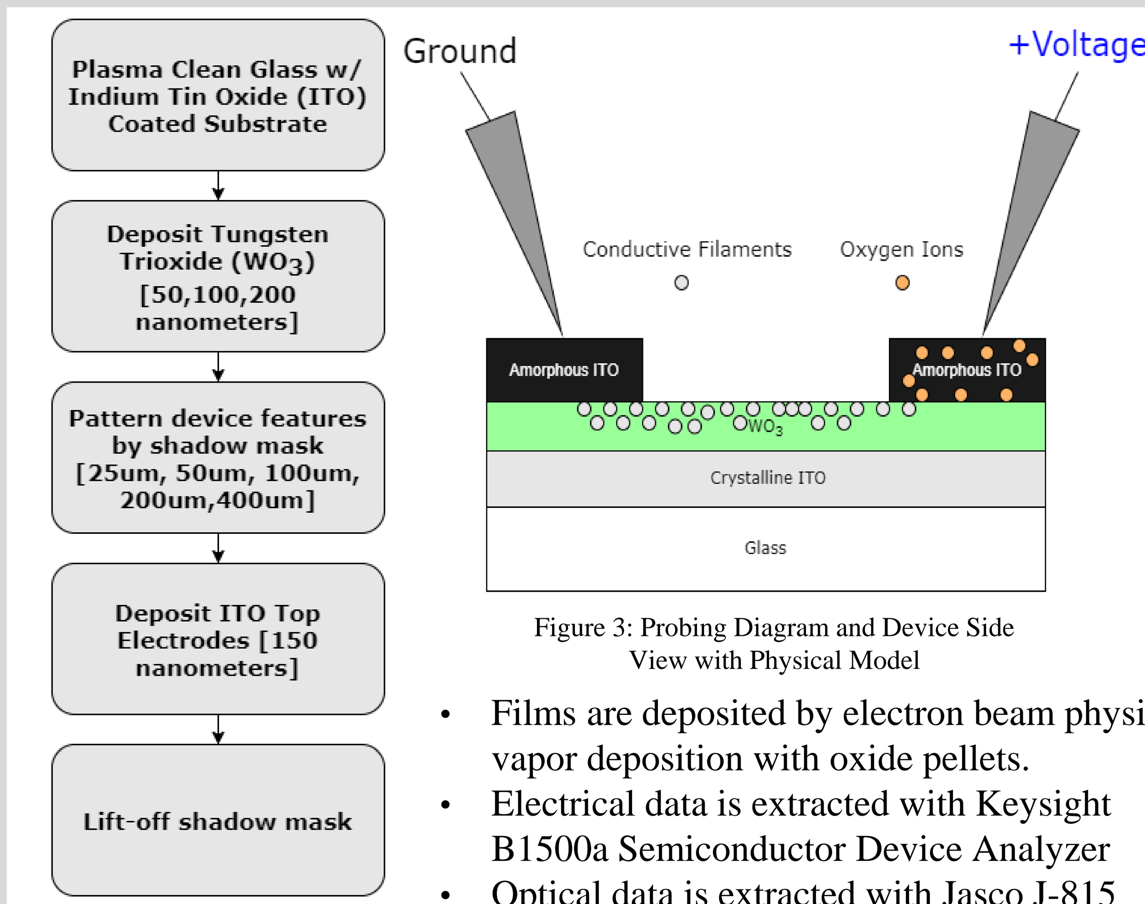

Figure 3: Probing Diagram and Device Side View with Physical Model

Figure 2: Fabrication Procedure

- Films are deposited by electron beam physical vapor deposition with oxide pellets.
- Electrical data is extracted with Keysight B1500a Semiconductor Device Analyzer
- Optical data is extracted with Jasco J-815 Spectrometer

Figure 4: Physical Vapor Deposition Chamber

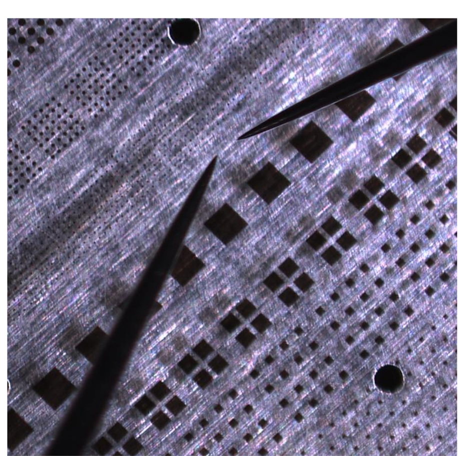

Figure 5: Top-Down View from Probe Station CCD. This view shows (from top to bottom) the 50um and 25 um Circle, and the 400 um, 200um, 100um, and 50um square feature sizes

Electrical Results

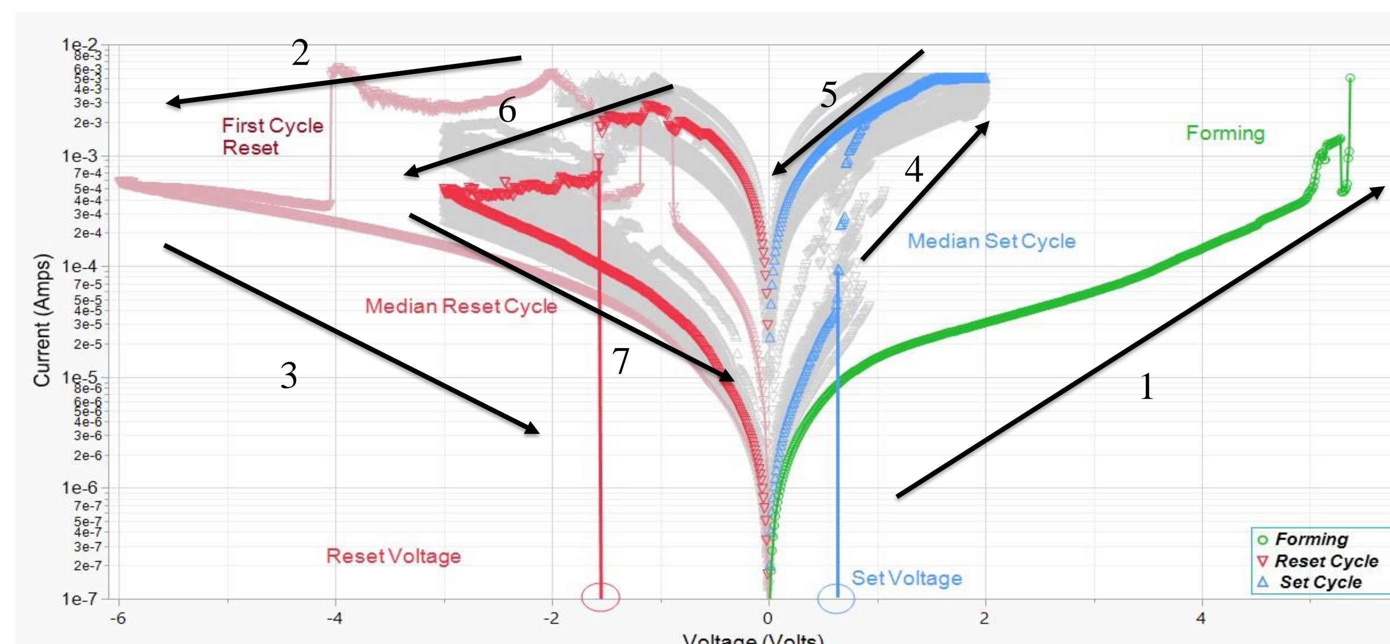

Figure 6: Current vs Voltage with Order of Voltage Sweeps

First, the oxygen ions and corresponding vacancies are generated through a high voltage stress called electroforming, which leaves the device in the low resistance state (LRS). Next, the first reset voltage sweep (-6V) occurs and the oxygen returns to rupture vacancies, leaving the device in the high resistance state (HRS). Then, the set sweep (+2V) occurs, and liberated oxygen drifts to the ITO electrode once again, returning the device to LRS. The subsequent reset cycles are -3V sweeps. Finally, this memory switching process is repeated for 20 cycles.

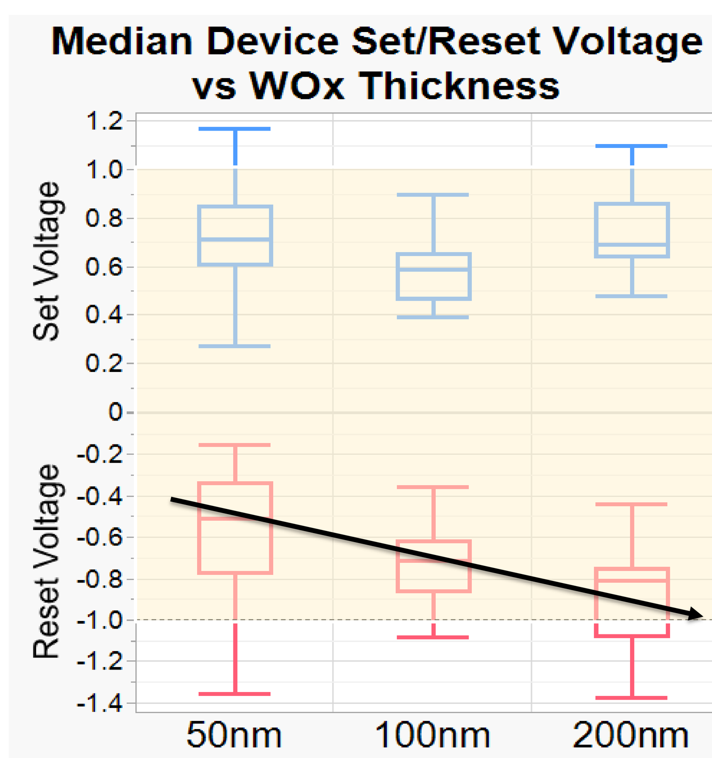

Figure 7: Median Set/Reset Voltages vs. Thickness

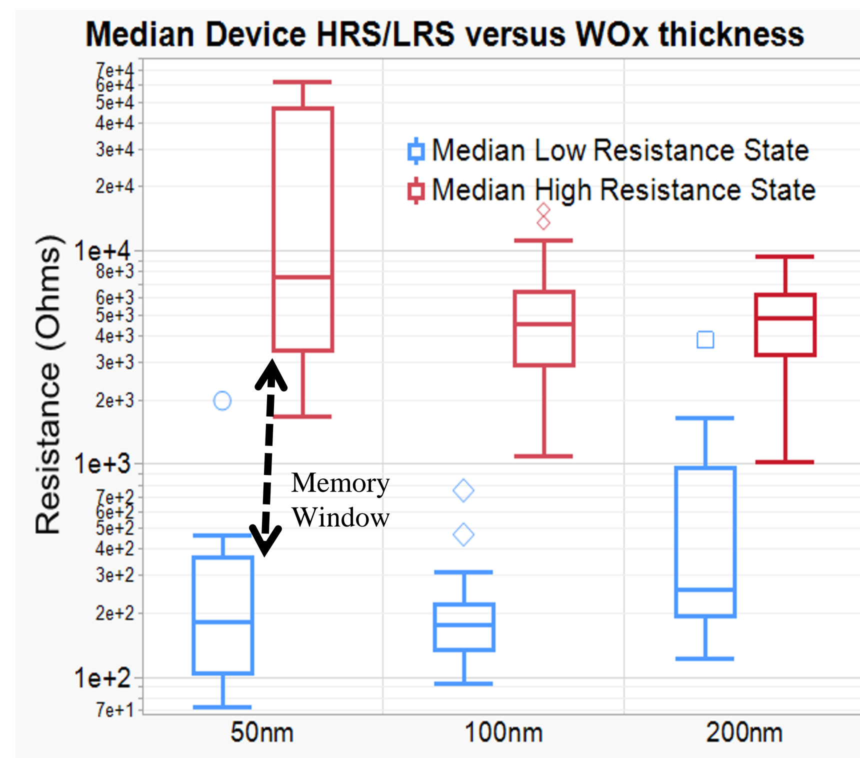

Figure 8: Median High/Low Resistance States

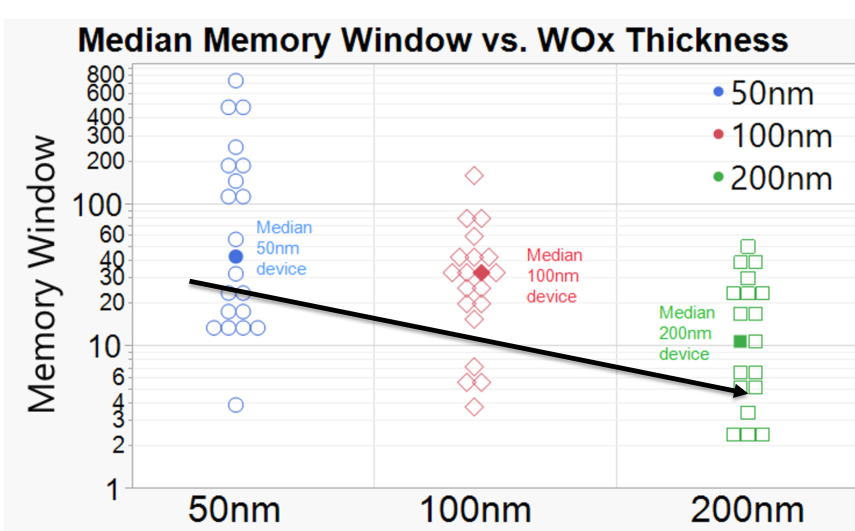

Figure 9: Median Memory Window vs. Thickness

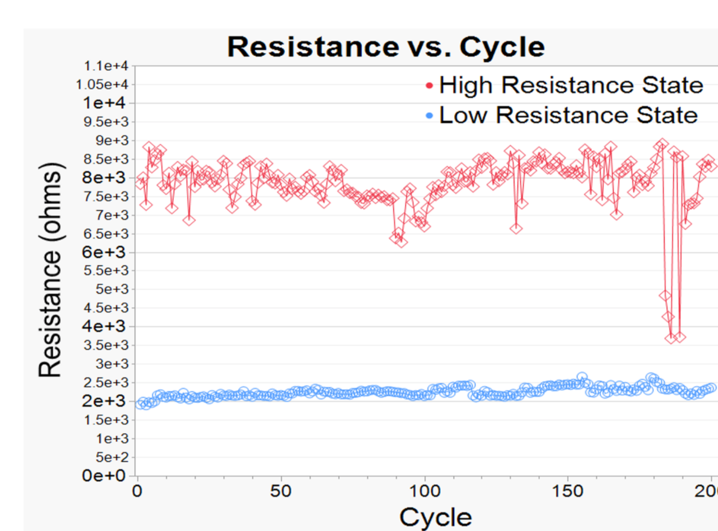

Figure 10: Endurance for 200 DC memory Cycles

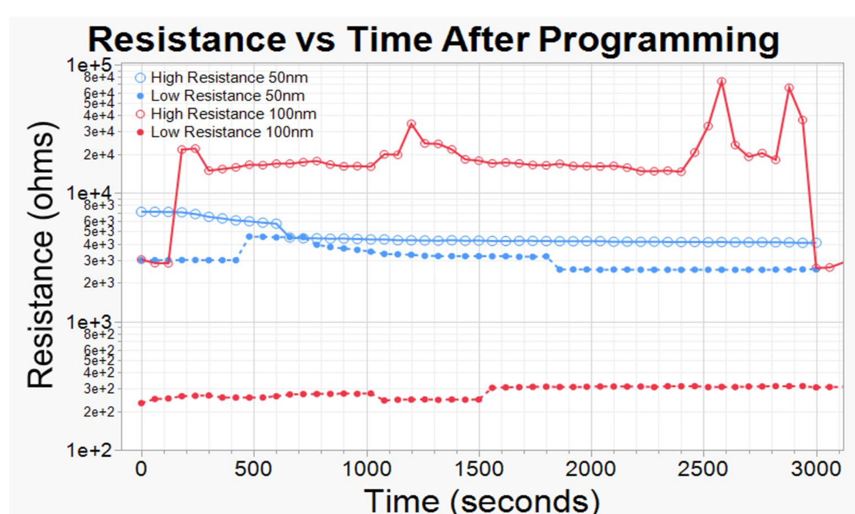

Figure 11: Retention After Programming

The majority of operation voltages lie within the +/-1V region. The variation in the high resistance state of the 50 nm device is the greatest among the three thicknesses. However, the best memory window is also seen in the 50 nm thickness. The only thickness that has overlapping resistance state box plots is the 200nm device, which makes the HRS/LRS ambiguous. High endurance is demonstrated by 200 DC memory cycles with no data drift. Retention characteristics require further investigation, but the two devices shown demonstrate the stochastic variation of state over a 1-hour period.

Optical Results

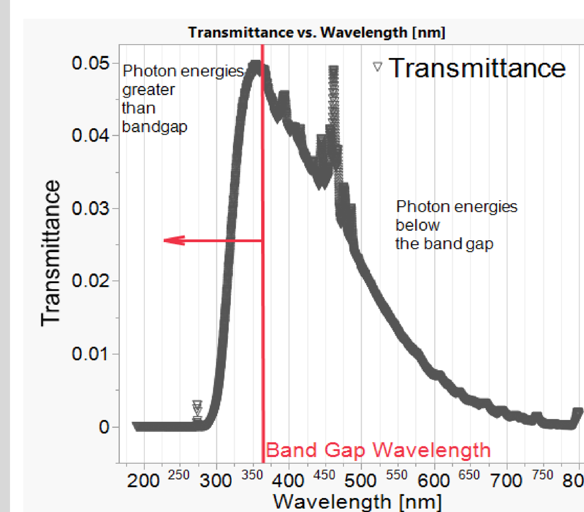

Figure 12: Endurance for 200 Cycles

Bouguer-Lambert Law

$$-\ln(T) = \alpha \cdot \text{Thickness}$$

α = absorption coefficent

Tauc's Relation

$$(\alpha \cdot h\nu)^{1/\gamma} = C(h\nu - E_g)$$

$\gamma = 2$ for direct allowed transitions

E_g = Energy Band Gap

1. Measured transmittance from visible to UV wavelengths.
2. Extracted absorption coefficient from transmittance.
3. Used Tauc's relation to construct a Tauc Plot.
4. Fitted linear region of Tauc Plot to an equation and extracted.

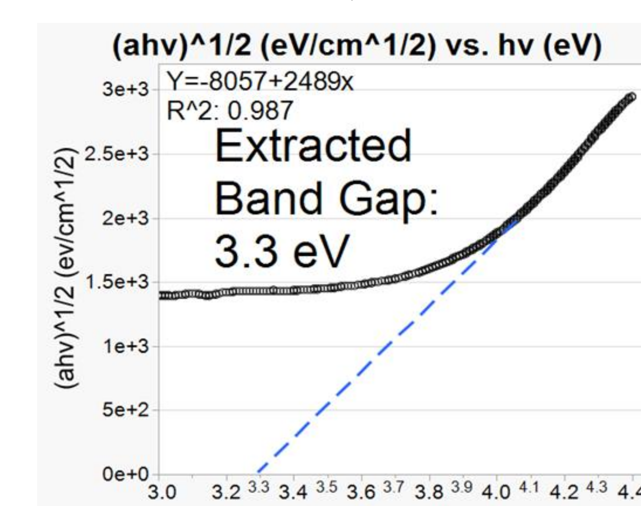

Figure 13: Tauc Plot for our WO_3

Conclusion

In this work, a WO_3 RRAM device with ITO electrodes fabricated by electron beam physical vapor is presented. We fabricated identical structures with multiple WO_3 thicknesses and compared their characteristics. First, the Set/Reset voltages are between +/- 1 Volt, which would keep the switching power of the device relatively low if it weren't for the low resistance. Next, a wide range of resistance states is shown at each thickness, with the largest variation shown in the 50 nm device. The LRS is on the order of hundreds of Ohms while the HRS is on the order of thousands of Ohms. The memory window is on the order of 10^1 to 10^2. A key trend is an inverse relation between Reset voltage and memory window with WO_3 thickness. As shown in figure 11, the devices suffer from poor data retention, within an hour the resistance state can vary greatly. However, this structure shows good endurance for 200 DC memory cycles (figure 10). In addition, UV-Visible spectroscopy was utilized to extract the band gap of our WO_3 (3.3eV), which is typical for room temperature deposited WO_3.

Future Work

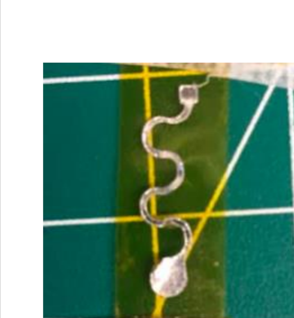

Figure 14: Flexible Substrate

One promising application of these memory devices is flexible memory. We have fabricated a flexible substrate, which enables the use of our technique for a planar deposition but will not be bound by a rigid substrate. This provides an opportunity to develop onboard memory for flexible electronic devices.

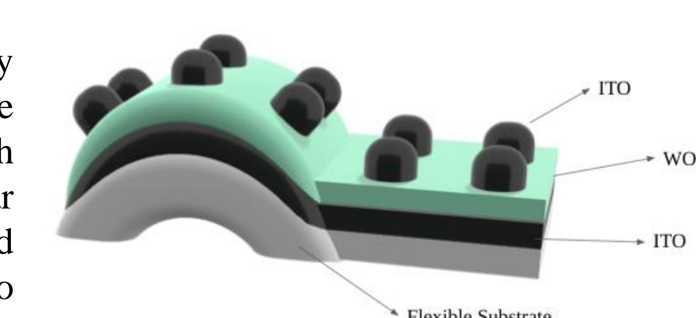

Figure 15: Flexible Memory Device Model

References

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