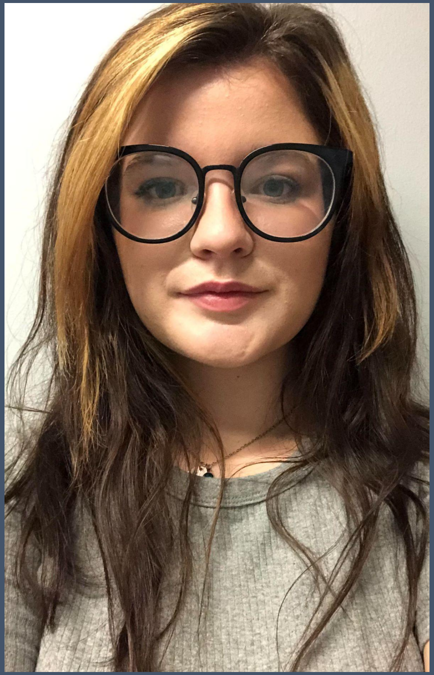
Semiconductor Research Capstone



SDRL

Semiconductors
and Device
Research Lab

Capstone 2021-2022

Jordan Beverly, Maxwell Weiss

Fall 2021-Spring 2022

NAU NORTHERN ARIZONA UNIVERSITY

College of Engineering, Informatics,
and Applied Sciences

Client Introduction

Principal Investigator: Dr. Ying Chen-Chen

Dr. Chen specializes in emerging memory technology looking specifically at Resistive Random Access Memory (RRAM). This has included research in low power self-selective crossbar resistive switching memory for high storage class memory applications, nanoelectronics fabrication, electrical characterization and physical modeling, next-generation memory devices for new computing architecture. Dr. Chen is currently the principal investigator of the Semiconductor Device and Research Lab at Northern Arizona University.

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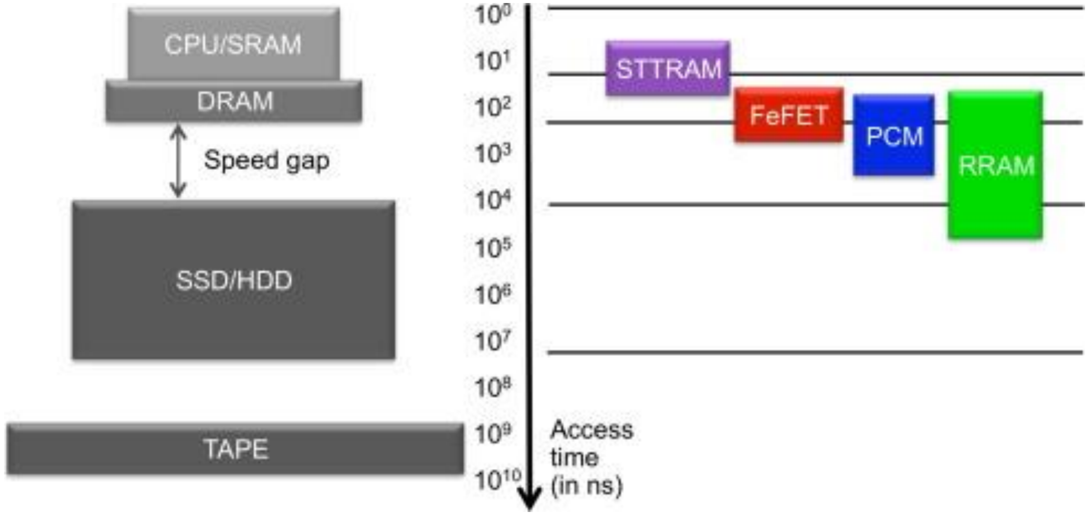
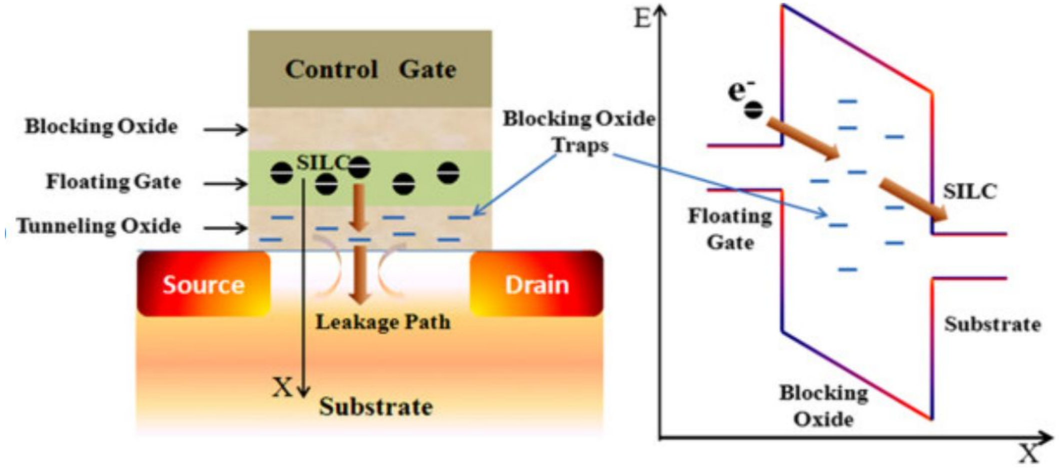
Motivation



There exists a speed gap between fast, volatile memories (i.e. DRAM,SRAM) and slow, non-volatile memory (i.e. Flash).



Transistor based Flash memory struggles scale down to smaller feature sizes due to increasing charge loss (i.e data loss).

We want to find the next generation memory to improve upon Flash *speed, reliability, and scalability*

Design of Experiments

Fabrication Requirements:

1. Fabricate Tungsten Oxide at three thicknesses [50nm, 100nm, 200nm] by e-beam vapor deposition
2. Use suitable electrodes that allow for resistive switching
   a) Pattern device features by shadow mask [25µm, 50µm, 100µm, 200µm, 400µm]

Testing Goals:

1. Demonstrate high endurance resistive switching
   a) 20 memory Devices (device to device variation)
      1. 20 memory cycles per device (cycle to cycle variation)
2. Extract memory characteristics from memory cycles
   a) High resistance state (HRS)/ Low resistance state (LRS)
   b) Memory window
   c) Set and Reset voltages
3. Reliability Testing
   a) Retention Testing
   b) Endurance Testing
4. Optical Spectroscopy from UV to Visible wavelengths

Design of Experiments

Resistive Switching Material:

Tungsten Oxide (WO_3)

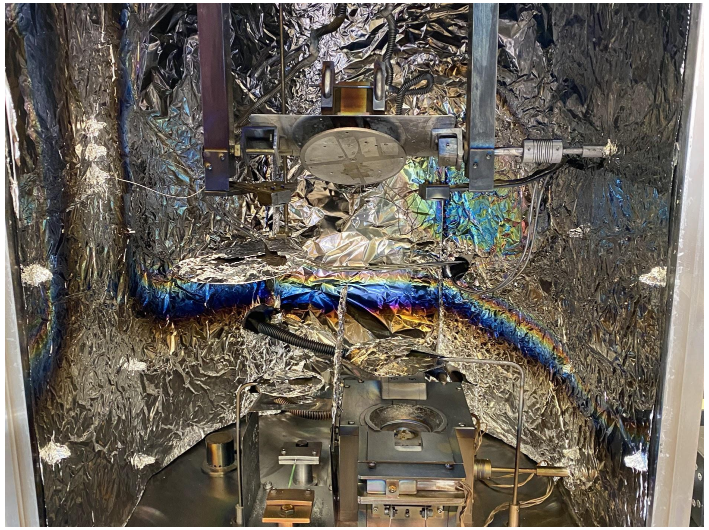
Electrode Materials:

Nickel (Ni)

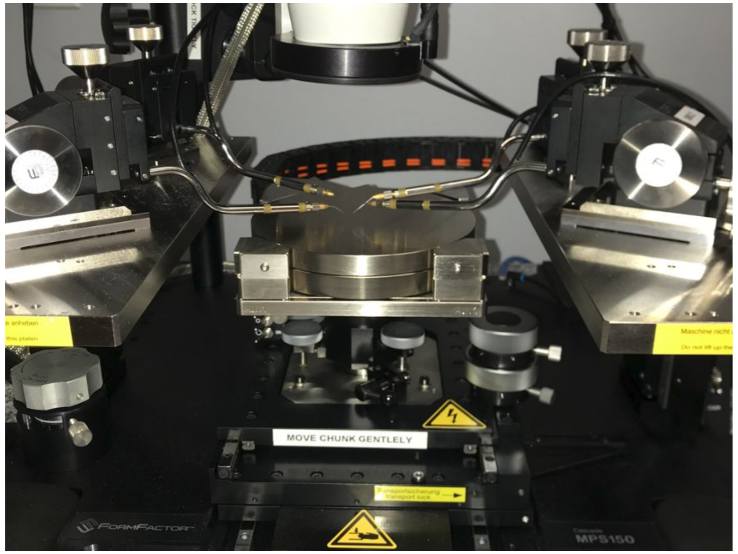
Indium-Tin Oxide (InO_3:SnO_2 90%:10% by weight)

Methods/Tools:

- **Electron Beam Physical Vapor Deposition(PVD) w/ mask lift off patterning**
- **Keysight B1500A Semiconductor Device Analyzer w/ Probe Station**
- **UV-Visible spectroscopy**



View inside PVD chamber. This is where samples are loaded.



View of probe station, this is where completed devices are electronically tested

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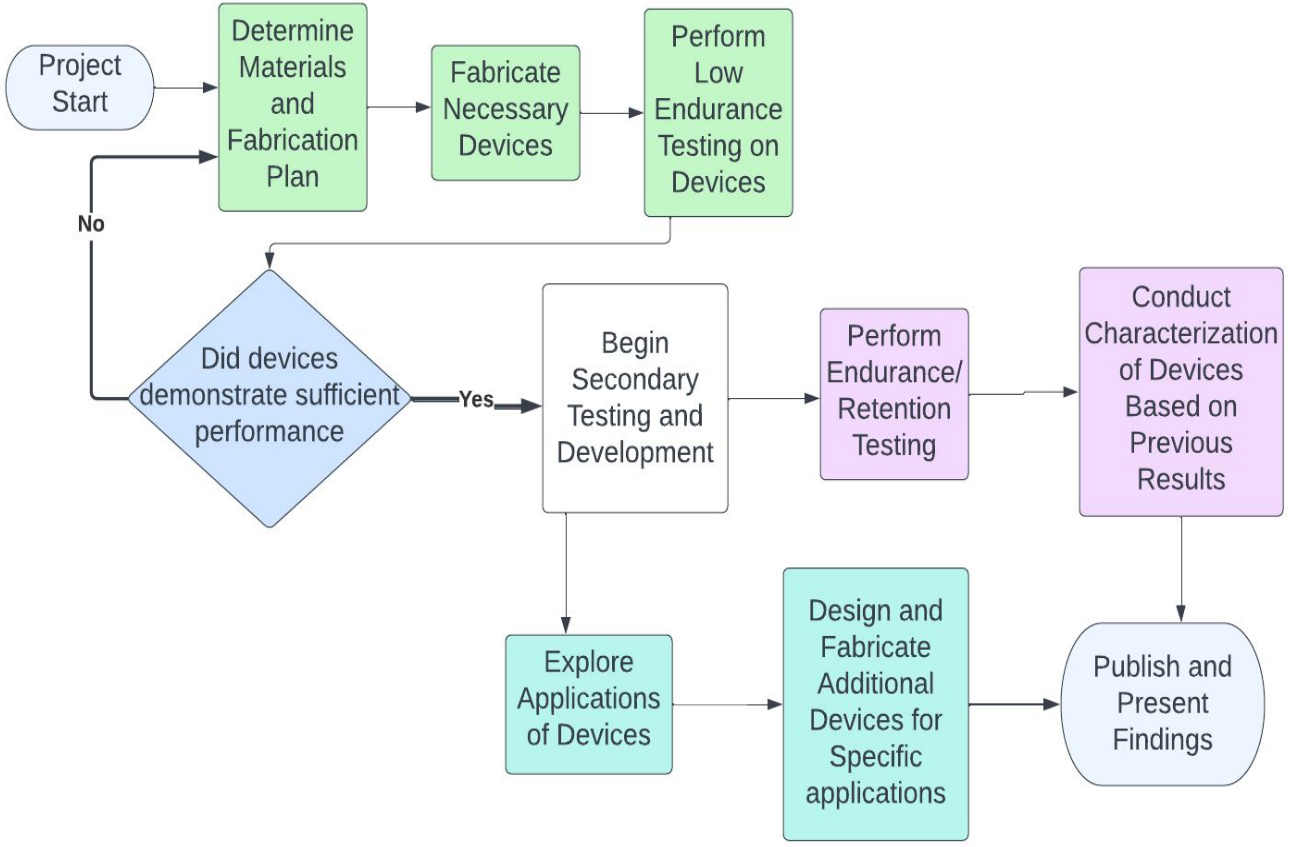
Approach


Project Start

Determine Materials and Fabrication Plan

Fabricate Necessary Devices

Perform Low Endurance Testing on Devices

Did devices demonstrate sufficient performance

No

Yes

Begin Secondary Testing and Development

Perform Endurance/ Retention Testing

Conduct Characterization of Devices Based on Previous Results

Explore Applications of Devices

Design and Fabricate Additional Devices for Specific applications

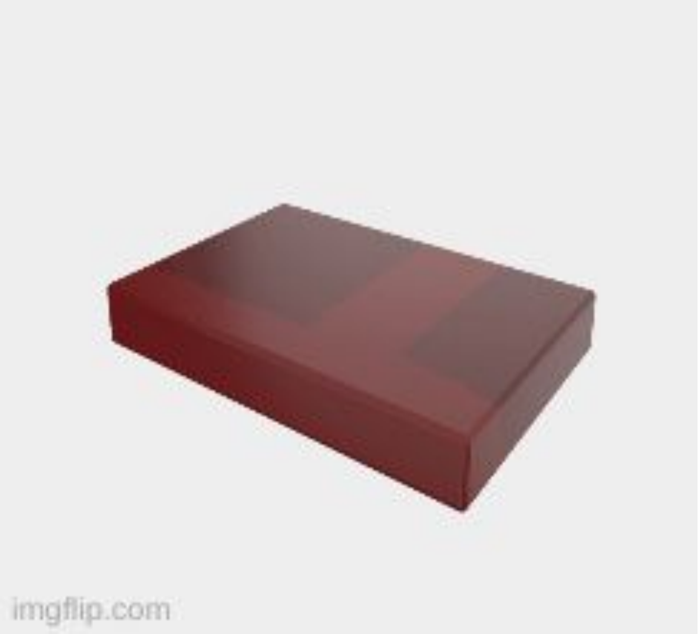
Publish and Present Findings

We began with nickel/WOx/nickel device structure, but these devices did not meet standards. We fabricated our next round of devices with ITO electrodes and they performed much better. After testing the low endurance cycling, we tested endurance and retention characteristics. Finally, we investigated tertiary applications and optical properties.

Fabrication Procedure

Nickel/WOx/Nickel

- Plasma Clean SI substrate
- Deposit Nickel
- Pattern device feature sizes by shadow mask [25um,50um,100um,200um,400um]
- Deposit Tungsten Trioxide(WO3) [10nm,20nm,100nm]
- Deposit Nickel top electrodes [150nm]
- Lift-off shadow mask



ITO/WOx/ITO

- Plasma Clean Glass w/ Indium Tin Oxide (ITO) Coated Substrate
- Deposit Tungsten Trioxide (WO$_3$) [50,100,200 nanometers]
- Pattern device features by shadow mask [25um, 50um, 100um, 200um,400um]
- Deposit ITO Top Electrodes [150 nanometers]
- Lift-off shadow mask

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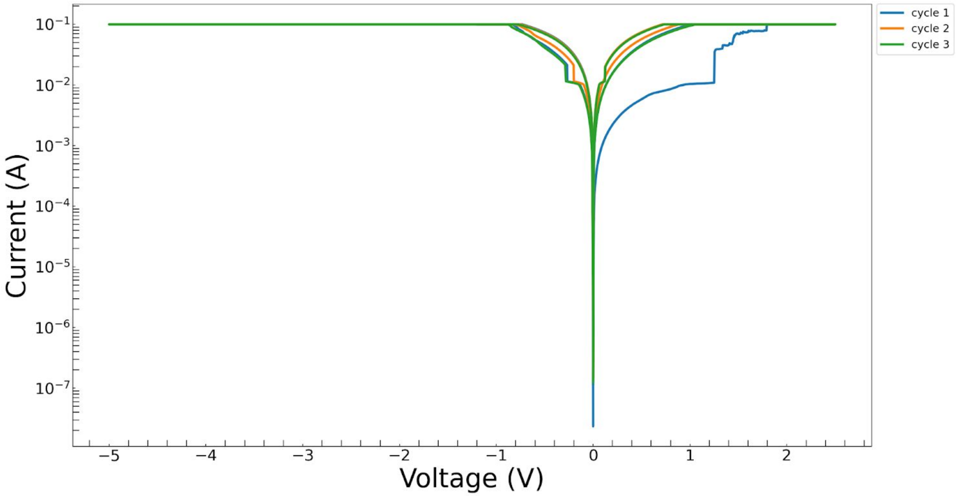
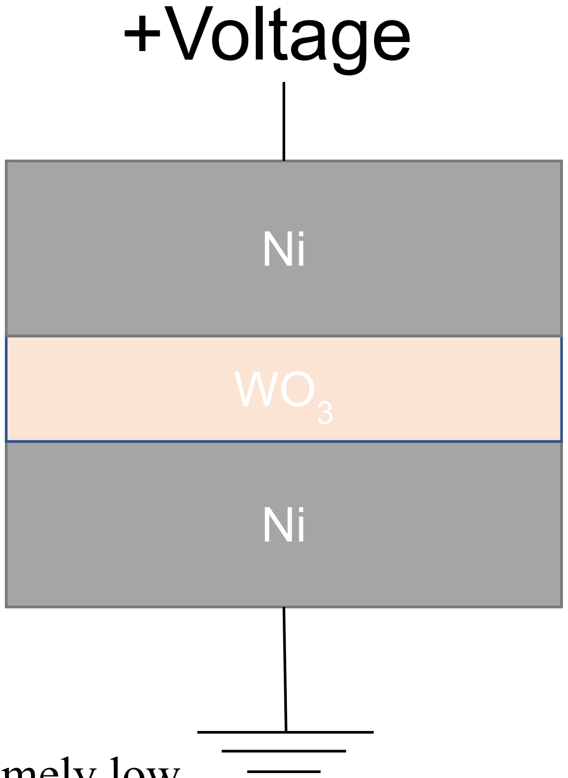
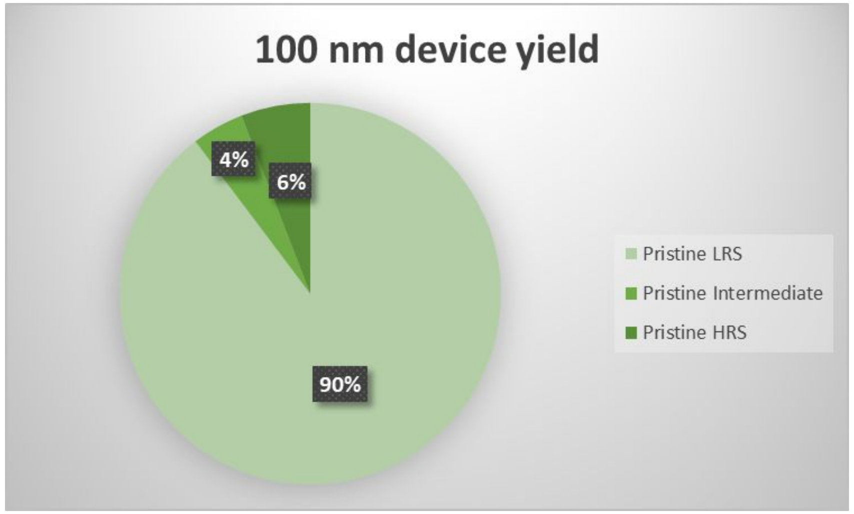
Nickel/WO_x/Nickel Results

The first structure we fabricated was the Ni/ WO_x/Ni composite.

After discovering that this structure could not demonstrate resistive switching, we switched to ITO electrodes.







- This current voltage curve demonstrates an extremely low resistance (<100 Ohms)
- Dual Nickel electrodes prevent resistive switching.
- A subsequent literature review shows that RRAM needs a noble (non-oxidizable metal) and an oxidizable metal to induce resistive switching.

H. . -S. P. Wong et al., "Metal–Oxide RRAM,"

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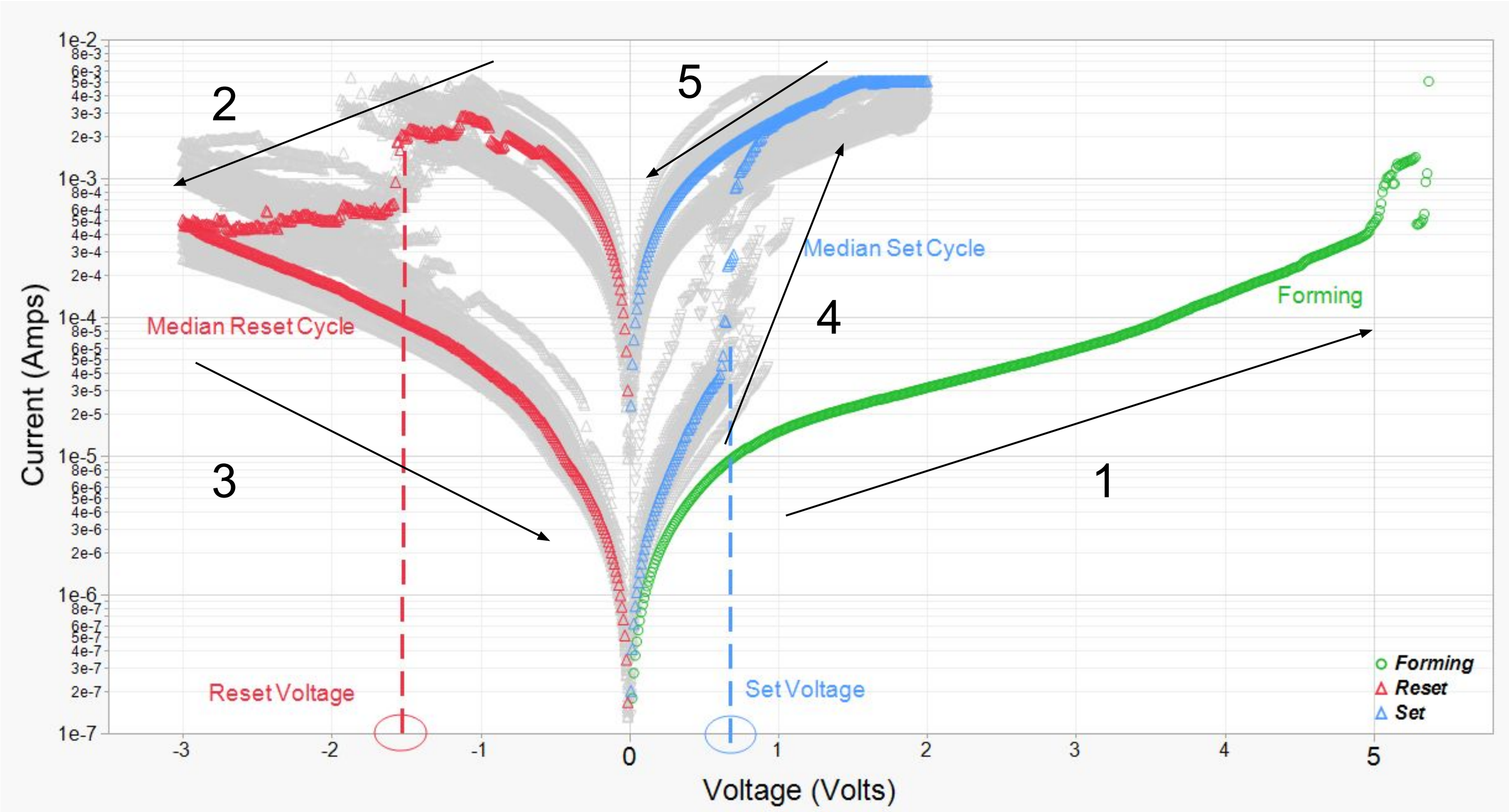
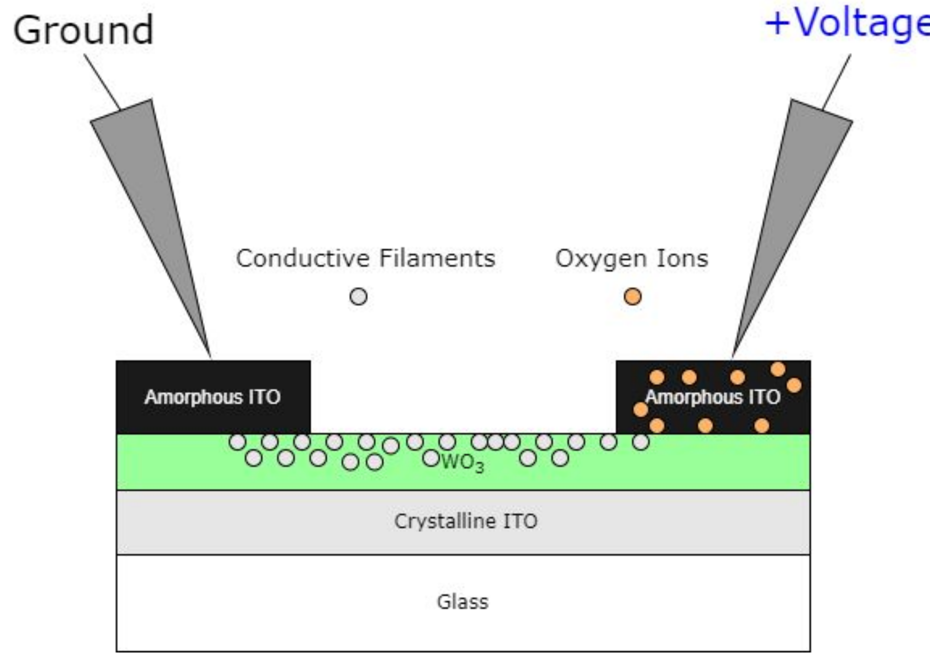
ITO/WO$_x$/ITO Results





1. Forming (As deposited->LRS)
2. Reset forward sweep (LRS->HRS)
3. Reset reverse sweep (HRS)
4. Set forward sweep (HRS->LRS)
5. Set reverse sweep (LRS)

LRS=Low Resistance State
HRS=High Resistance State

Conductive Filament Theory

Electroforming: Form the percolation path (soft-breakdown).

Reset: Oxygen ions (O^{2-}) drift back and oxidize

Set: Generation oxygen vacancies (V_O^{2+})

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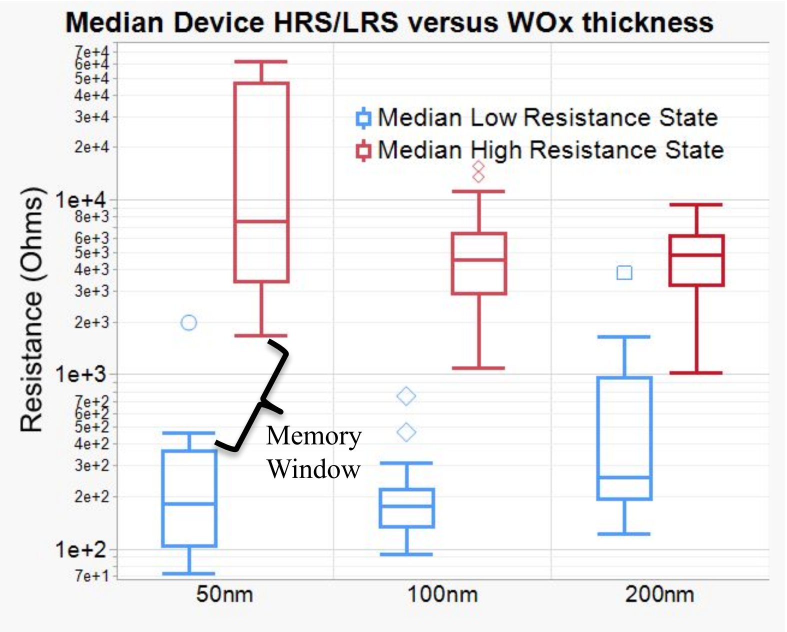
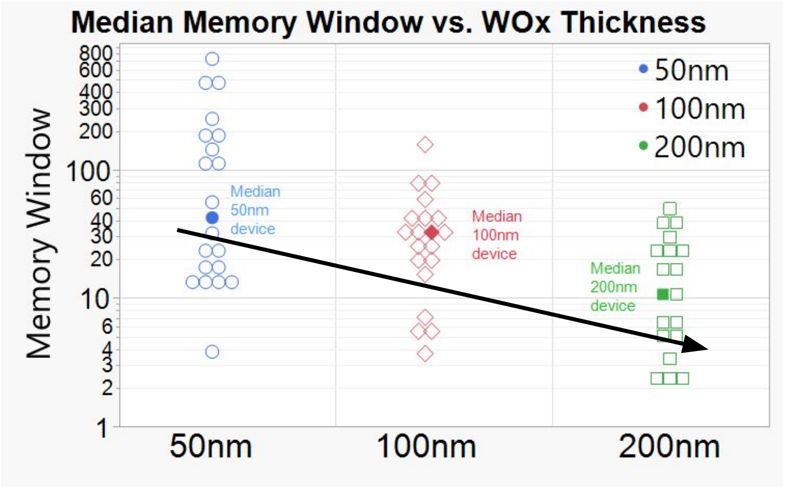
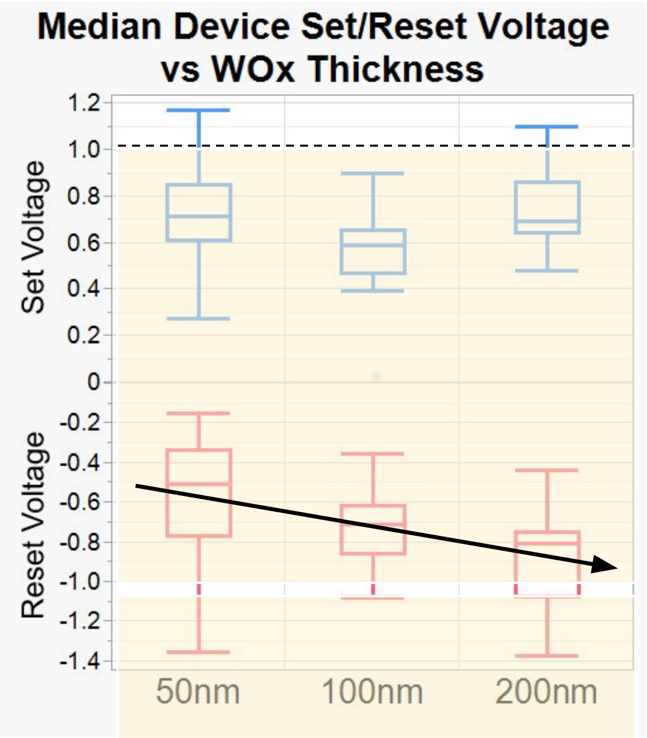
Memory Cycle Data



Median Device HRS/LRS versus WOx thickness



Median Memory Window vs. WOx Thickness



Median Device Set/Reset Voltage vs WOx Thickness

- Memory Window increases with decreasing thickness.
- Operation voltage are below +/-1V (SET/RESET) for low power applications.

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Unpublished results, paper in progress

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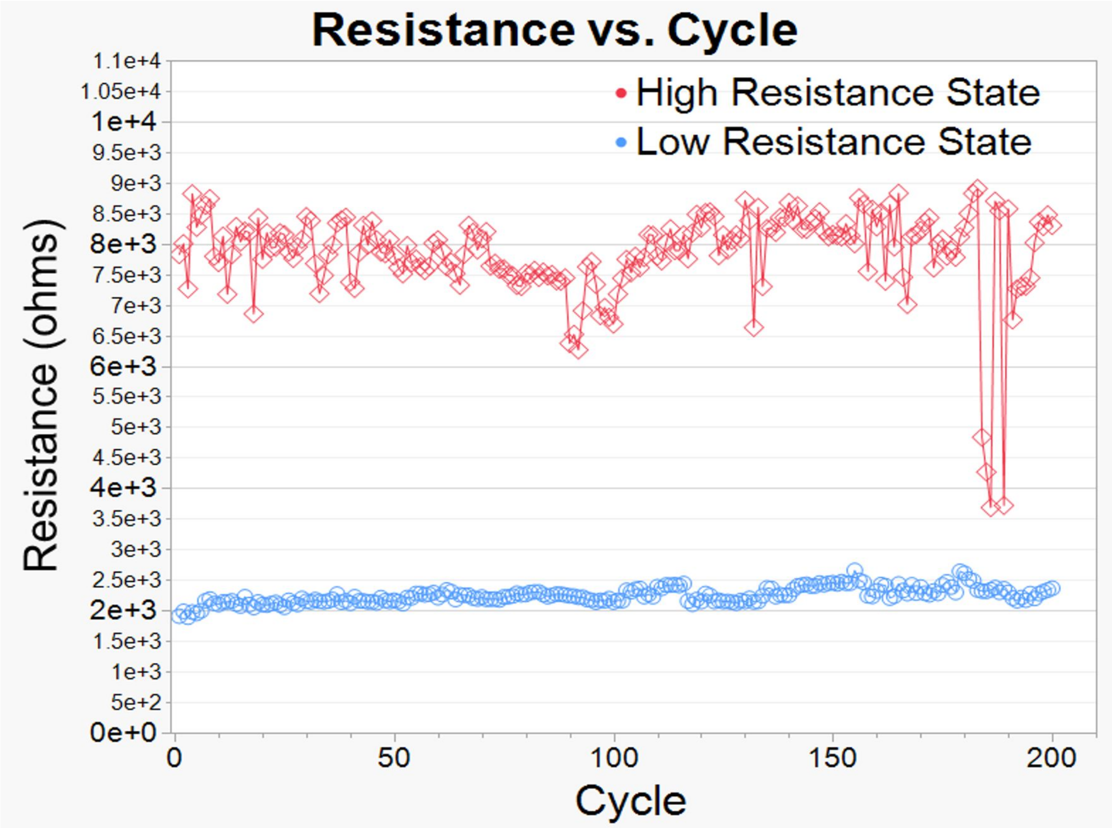
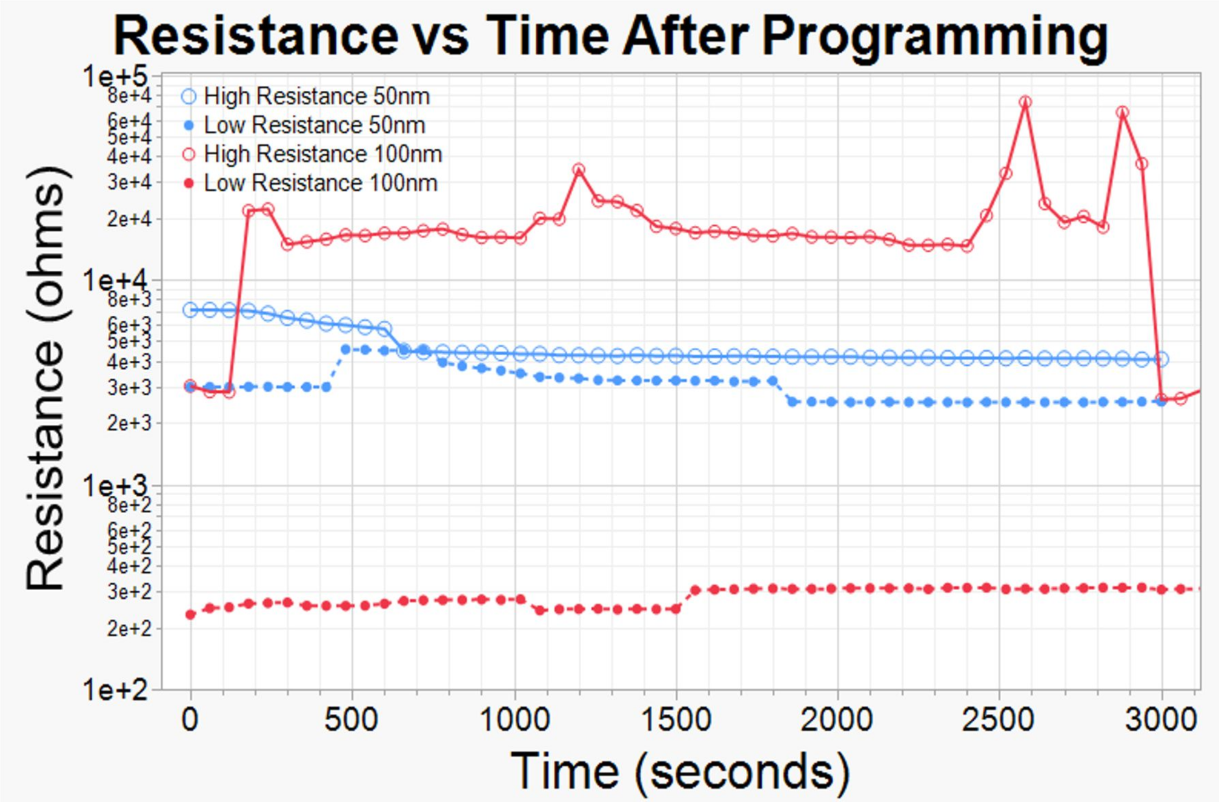
Reliability Testing





- **Endurance up to 200 cycles demonstrated**

- **Retention is poor**
- **Random fluctuations in high resistance state over 1 hour**

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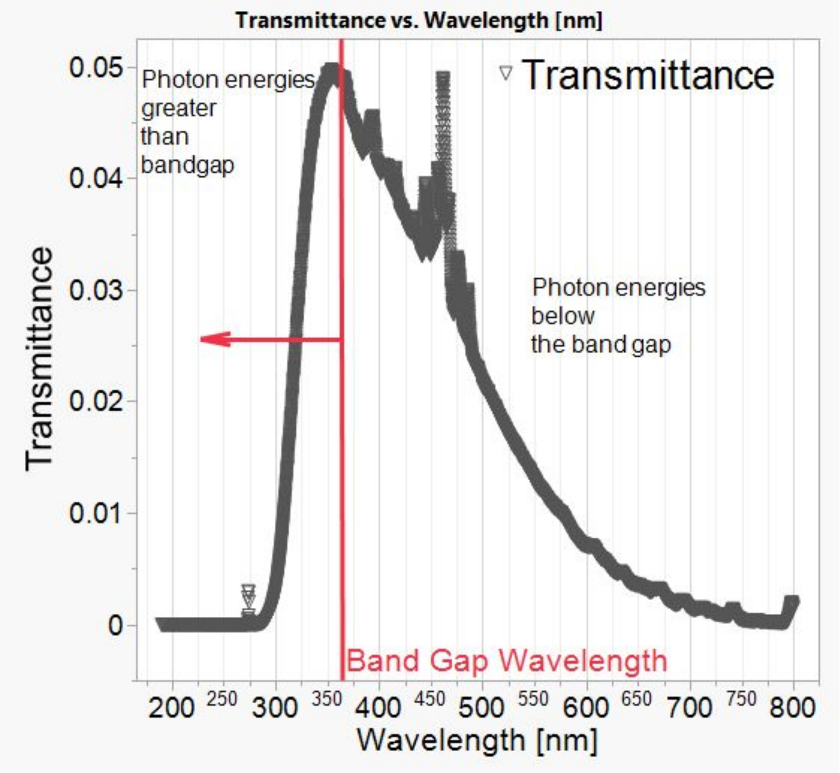
Spectroscopy Results



Photon energies greater than bandgap

Photon energies below the band gap

Bouguer-Lambert Law

$$-\ln(T) = \alpha \cdot \text{Thickness}$$

α = absorption coefficient

Thickness=50nm

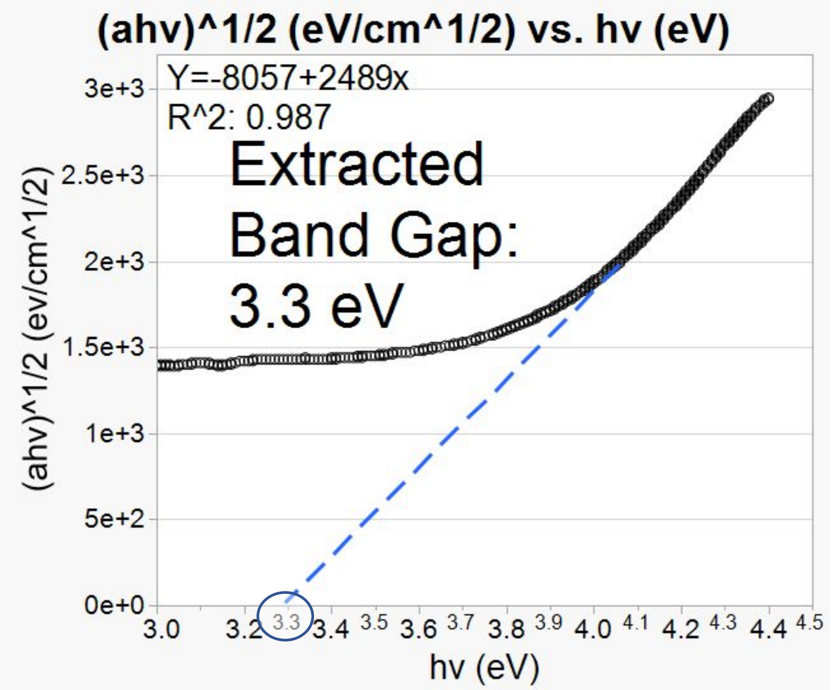
Tauc's Relation

$$(\alpha \cdot h\nu)^{1/\gamma} = C(h\nu - E_g)$$

α = absorption coefficient

E_g = Energy Band Gap

R. Sivakumar, *et. al.* Optical Materials, Volume 29, Issue 6, 2015



Y=-8057+2489x

R^2: 0.987

Extracted Band Gap: 3.3 eV

Annealing Observations

- At heats >250 Celsius ITO will anneal into a polycrystalline phase.
- In this phase, ITO is transparent to visible wavelengths
- Under high electrical currents Joule heating occurs and the ITO can undergo annealing

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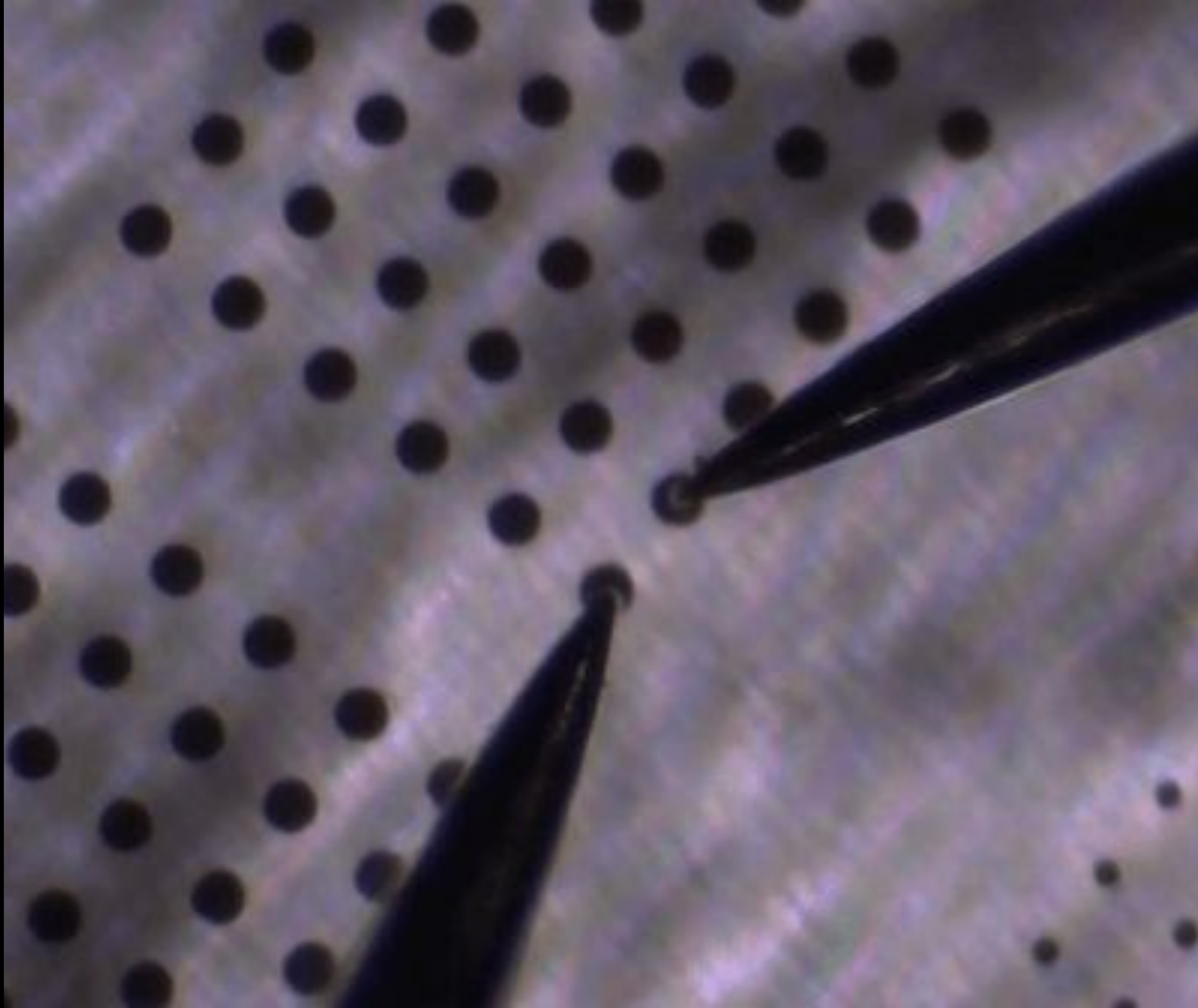
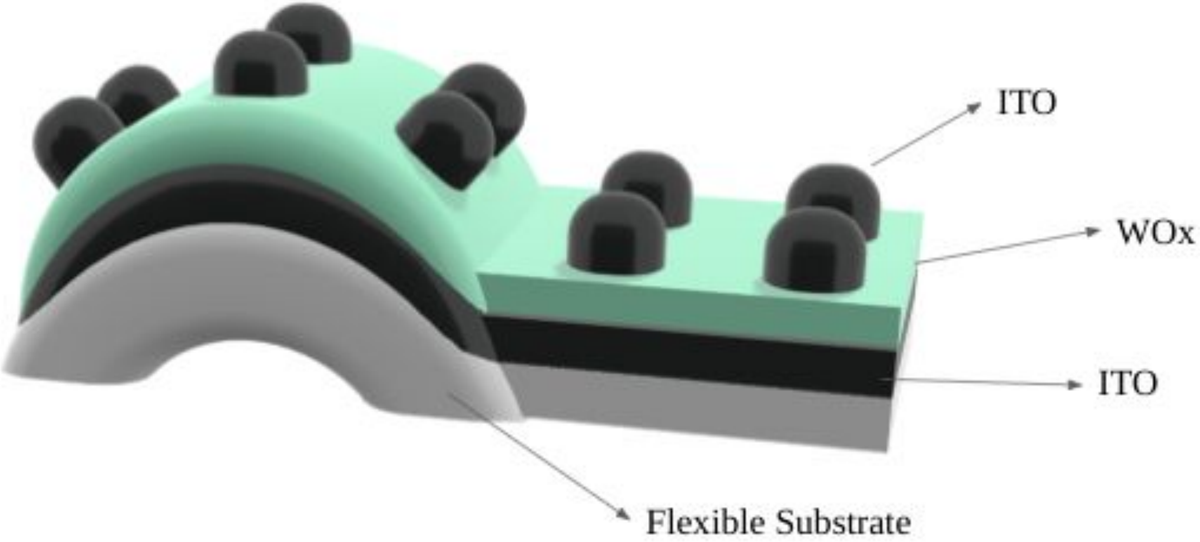


Future Work

- Further ITO/WOx/ITO research
  - Compare planar ITO/WOx/ITO to vertical
  - Utilize X-ray photoelectron spectroscopy and Energy Dispersive Spectroscopy to analyze material properties.
- Flexible Memory
  - The same fabrication methods done for this work can be done on a flexible substrate. This would provide a path for the development of onboard memory for flexible electronics



Proposed Flexible Memory model

Fabricated flexible substrate

Challenges

- First device round fabrication issues
  - Deposition machine failed two times which slowed progress
  - Entire weeks progress halted due to need to replace foil
- Device structure prohibited successful probing
  - Probing edgeless devices twisted the probe tip so we couldn’t test with that method.
  - Getting a good ground probe by poking through the WOx made testing procedure arduous and uncertain.
- Experiment design structure halted productivity
  - Should have thoroughly tested first device after fabrication.
  - Should have researched electrode materials and the necessity of noble electrode first.

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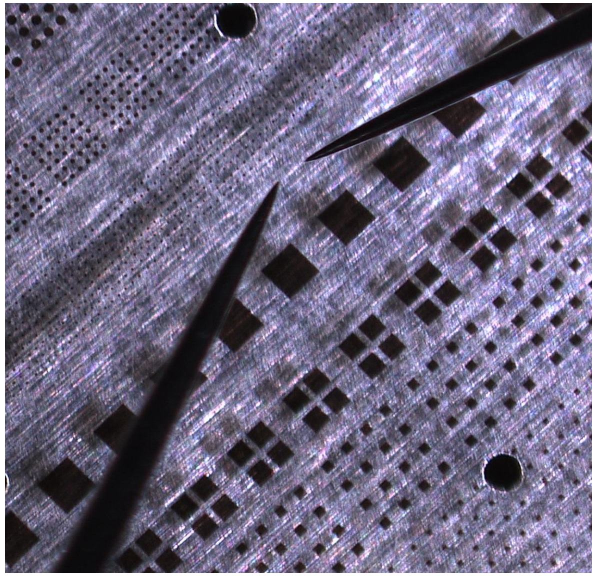
Conclusion

- Set/Reset Voltages of device lie between +/- 1V.
  - Reset voltage is lower for smaller WOx thickness
- Low resistance states vary around 500 Ohms
- High resistance states lie near 1.5 kOhm to 10 kOhm.
- Memory window is 10^1 -10^2 .
  - MW decreases with increasing thickness
- Devices can endure 200 cycles.
- Devices demonstrate poor data retention over an hour.
- Absorbance spectroscopy confirms that band gap is 3.3eV.



Top-Down View from Probe Station CCD. This view shows (from top to bottom) the 50um and 25 um Circle, and the 400 um, 200um, 100um, and 50um square feature sizes

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Thank you for your time!

Do you have any questions?