

Subject: Testing Report Document

Among the emerging memories, Resistive Random Access Memory (RRAM) is a promising candidate to bridge the memory wall between CPU and memory. The purpose of this work is to explore the resistive switching behaviors of Tungsten Oxide (WO_x). The memory devices were fabricated using electron beam physical vapor deposition and a lift off process with a shadow mask. The Tungsten Oxide deposition occurred at varying thicknesses, followed by Indium Tin Oxide (ITO) electrodes as the transparent conductive electrodes. Unlike traditional engineering projects, the goals (i.e requirements) of the project changed as new results were found.

The tests for this project can be divided into electrical and optical tests. The methods of both tests will be described in detail later. There were 3 types of electrical tests performed, memory cycling, endurance, and retention. Memory cycling was performed on 60 devices total (20 devices per WO_x thickness) with 20 memory cycles per device. Endurance was performed on 2 different thicknesses, retention was performed on two different thicknesses. The memory cycling took 1 month with about ~50-60 hours of testing. Endurance took 2 hours. Retention testing took 4 hours. Optical testing took 3 hours total. Electrical results were placed into box plots primarily due to statistical variation among 60 devices. Optical testing was a form of absorbance spectroscopy.

Introduction:

The purpose of this project is to develop an emerging memory device which enables the storage and high operation speed for the high demands of current computing applications in the area of microelectronics. The Tungsten Oxide (WO_x)-based RRAM presented in this work as an active layer with its area effect and thickness effect as key analysis parameters. Moreover, its endurance and retention abilities are investigated as well as the device-to-device and cycle-to-cycle variation within each feature size. In addition, UV-visible spectroscopy was utilized to study the optical properties of WO_x-based RRAMs. The WO_x-based RRAM has also been developed with soft materials and new design, which explores the feasibility towards novel flexible memory applications and electronics systems. The physical modeling on WO_x-based RRAM is investigated with the electrical and optical characterizations by semiconductor analyzer and spectrometer.

System Architecture:

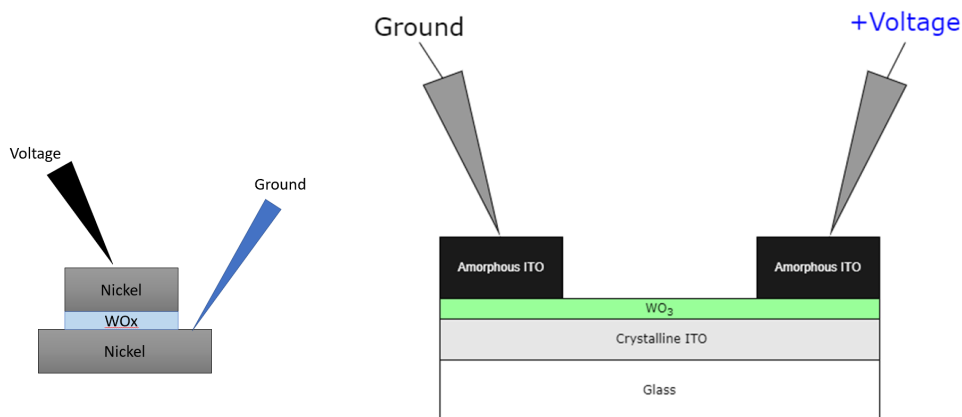


Figure 1: Side view of device with probe tips shown (3 thicknesses for each structure: 50,100,200 nanometers)

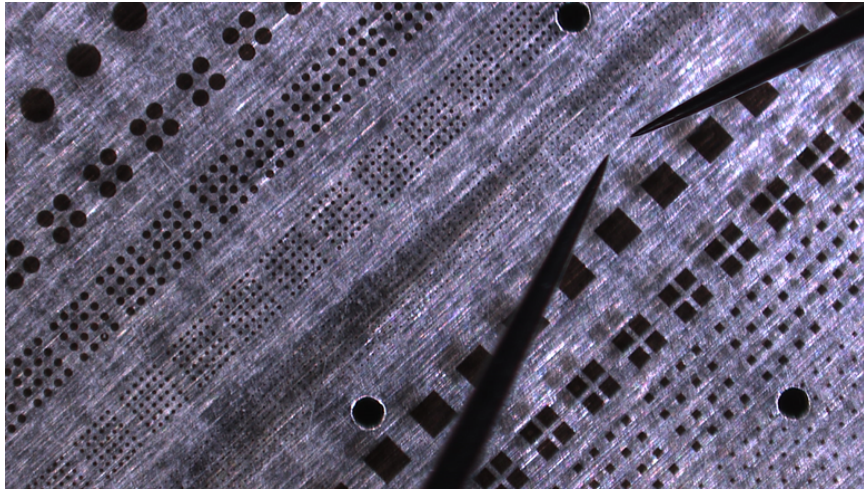


Figure 2: Top down view of devices from probe station camera

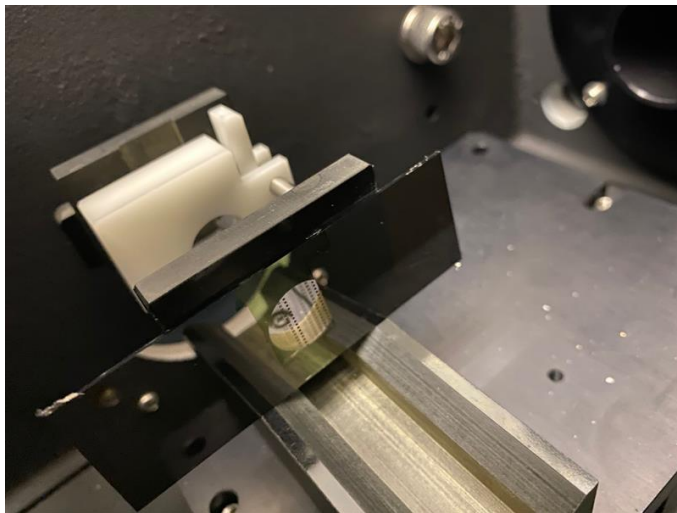


Figure 4: Optical Spectrometer setup

Testing architecture:

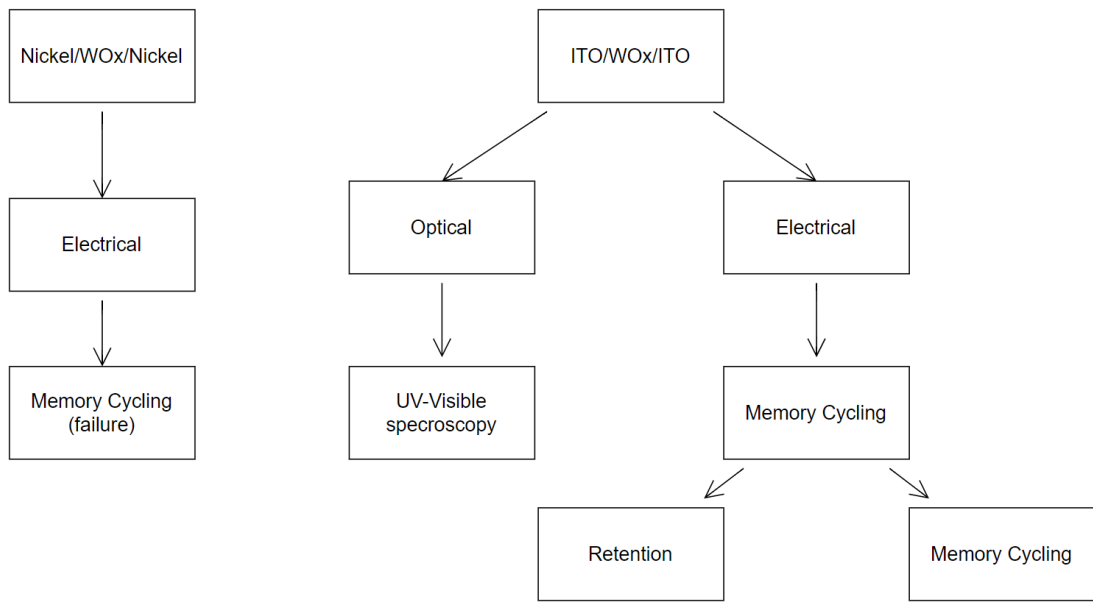


Figure 5: Testing Architecture

Requirements:

Type of Test	Status	Req #	Requirement
Fabrication		1	Top electrode thickness must be greater than 100nm but less than 200nm.
		1.1	Active Layer must be fabricated at different thicknesses: 10nm 20nm 100nm thicknesses.
Material		2	Electrode material must be Nickel or ITO
		2.1	Active layer must be WO3
		2.2	All material properties may be verified with Energy Dispersive Spectroscopy- line scan.
Deposition		3	Vacuum Pressure must be below 9.99×10^{-6} Torr when doing vapor deposition.
		3.1	Deposition rate must be recorded.
		4	Multiple devices must be tested.
		4.1	Different feature Sizes
		4.1.1	100um, 50um, 25um
Electrical		4.2	For each feature size and thickness 20 devices must be tested, and data must be compared to evaluate Device to Device (D2D) variation
	*	4.3	For each feature size and thickness 20 switching cycles must be performed to evaluate cycle to cycle (C2C) variation.
		4.4	Memory Performance Testing
	*	4.4.1	I-V Curves
		4.5	MLC Testing
	*	4.6	Endurance testing 10^9 Cycles
	*	4.7	Retention Testing 10^{12} seconds (extrapolated)
Characterization		5	Characterization Requirements
		5.1	Fit to mathematical conduction models
		5.2	Extraction of barrier height
		5.3	COMSOL Model
Optical Test		6	UV-Visible Spectroscopy
	*	6.1	UV-Visible spectroscopy on ITO devices at each thickness at each stage of the fabrication
		6.2	Annealing of ITO to induce transparency in the visible wavelengths
		6.3	Extraction of band gap from absorbance

Major Requirements:

1. 20 devices for each thickness

It is essential to test 20 devices at each thickness to see the device to device variations.

2. 20 cycles for each device

By performing 20 cycles on each device it ensures that statistical variations are taken into account for each device.

3. Endurance and Retention testing

Endurance and retention testing are important because they ensure that the memory cells are capable of a large number of cycles and that they retain the data for a long time after programming.

Types of Test:

1. Unit Test Step-By-Step: ITO/WO_x/ITO Memory Cycling
 - a. 20 memory switching cycles.
2. Unit Test Step-By-Step/Matrix: Ni/WO_x/Ni Memory Cycling
3. Unit Test Matrix: ITO/WO_x/ITO memory cycling at different thicknesses
 - a. 20 devices at each thickness (50nm ,100nm ,200nm)
4. Unit Test Matrix: ITO/WO_x UV-Visible spectroscopy at different thicknesses

Major Tests:

1. ITO/WO_x/ITO memory cycling (Step by step and Matrix)

This was the primary form of testing for our project, and thus most of the results come from this type of testing. The results are shown in the Appendix figures 6 through 11. Figure 6 is a typical memory cycle where forming, set, and reset are shown, this is the step by step test. First the device is put through a forming sweep with a high voltage stress with a current limit at 5mA in

which the device enters a low resistance state. Then, a negative voltage sweep to -6V is performed where the device transitions back to a high resistance state. This first reset stop voltage of -6V is different from subsequent reset cycles where the stop voltage was -3V. Finally, the set sweep of 2V with a current limit at 5mA switches the device back to the low resistance state. The subsequent figures 7-9 show the results of the matrix test where we performed the memory cycling for three different thicknesses.

2. UV-Visible spectroscopy of ITO/WO_x

Figure 12 in the appendix shows the results of the UV-Visible spectroscopy. This was originally a matrix test in which the spectrum was taken for the three different thicknesses. However, the results were all the same so the 50nm spectrum was used for the analysis.

Analysis of Results:

Figures 7-9 show the key memory characteristics of the ITO/WO_x/ITO. From figure 7 it is evident that the resistance states have a high degree of variation. No noticeable trends are seen in the resistance states versus thickness other than the fact that the 50nm states have the highest variation. This leads to figure 9 memory window plot (memory window is the difference between high resistance and low resistance state). The highest memory window is seen in the 50nm device. The trend shows that the memory window decreases with increasing WO_x thickness. The set/reset voltage box plot has similar variation to the resistance states, but with the trend that the reset voltage decreases with increasing WO_x thickness. A key performance parameter is that the majority of the set/reset voltages are between +1V and -1V.

Figure 12 illustrates the transmittance of ITO/WO_x from the UV-Visible wavelengths. Using this data, the thickness of the WO_x, and Bouguer-Lambert law I was able to extract the

absorption coefficient. Using the absorption coefficient I was able to make a Tauc Plot in which the x-intercept of the linear region is the energy band gap (3.3eV) which is typical for WO_x deposited by physical vapor deposition at room temperature.

Figure 13 shows the results of Ni/WO_x/Ni memory cycling. It is evident that the devices have no resistive switching. We did not expect this result, but hypothesize that the lack of switching is due to the lack of an “oxygen reservoir” electrode. Because both electrodes are nickel it is possible that after forming, the oxygen ions and nickel are creating a nickel oxide and preventing Reset from ever occurring due to lack of free oxygen.

Lessons Learned:

From the results of the Nickel/WO_x/Nickel RRAM we concluded that nickel needed to be paired with an inert/noble electrode such as Platinum, Titanium or an oxygen reservoir electrode such as Titanium Nitride or Indium Tin Oxide. From this obstacle we learned that research goals can be quite different from traditional engineering projects. For example, after the failure of the nickel devices we switched to the ITO/WO_x devices and altered the design of our experiments entirely.

Appendix:

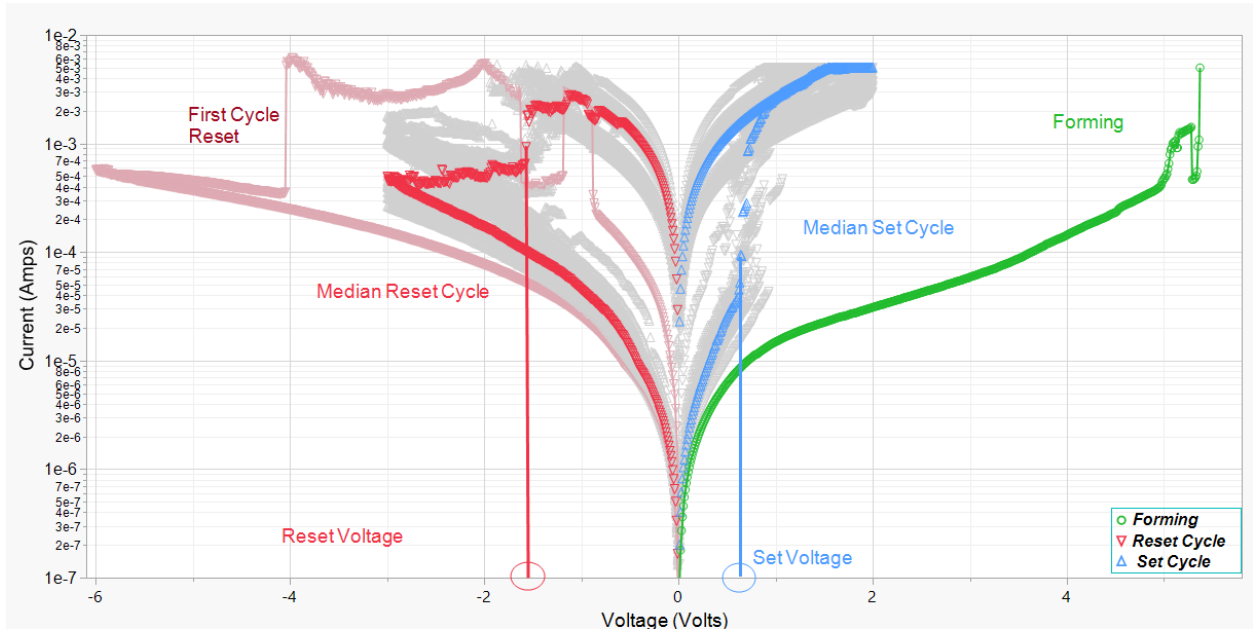


Figure 6: Typical I-V curve for a planar ITO/WOx/ITO device

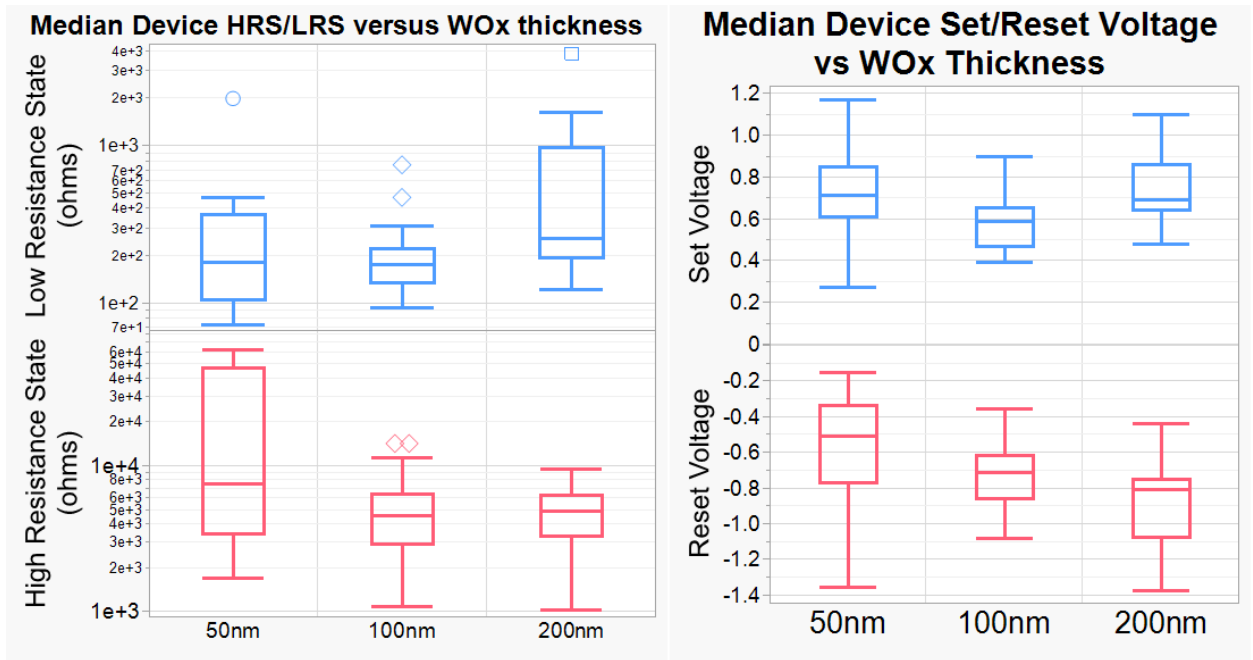


Figure 7: HRS/LRS box plots vs WOx Thickness Figure 8: Set/Reset voltage box plots

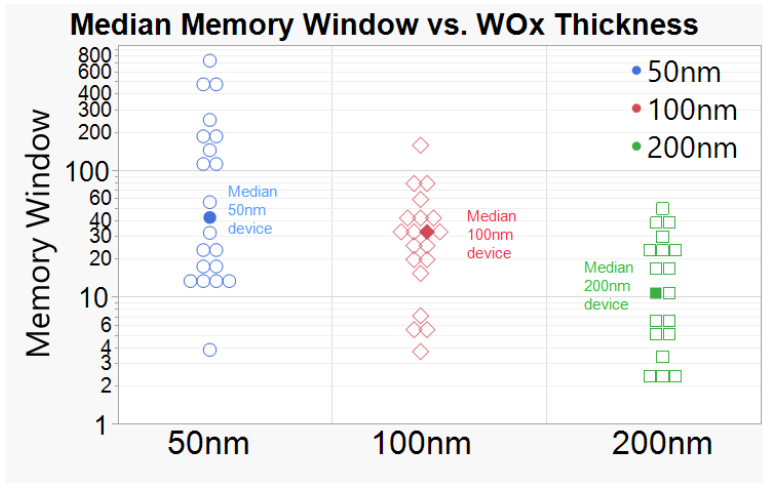


Figure 9: Memory Window vs. WOx Thickness

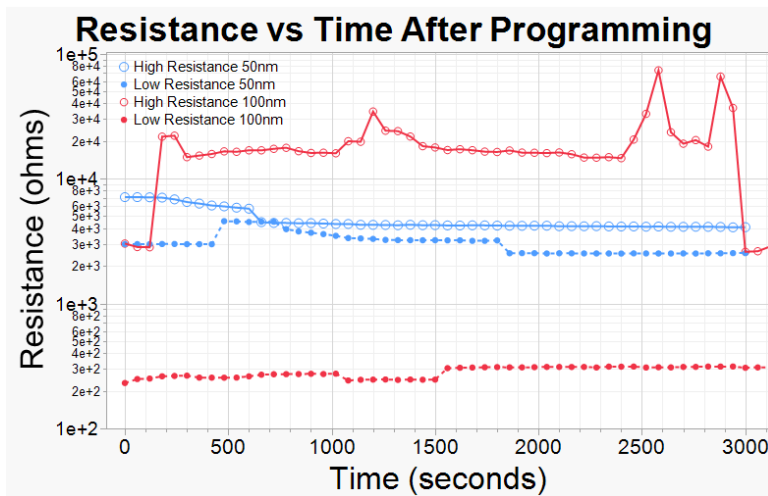


Figure 10: Retention Test (Resistance vs Time)

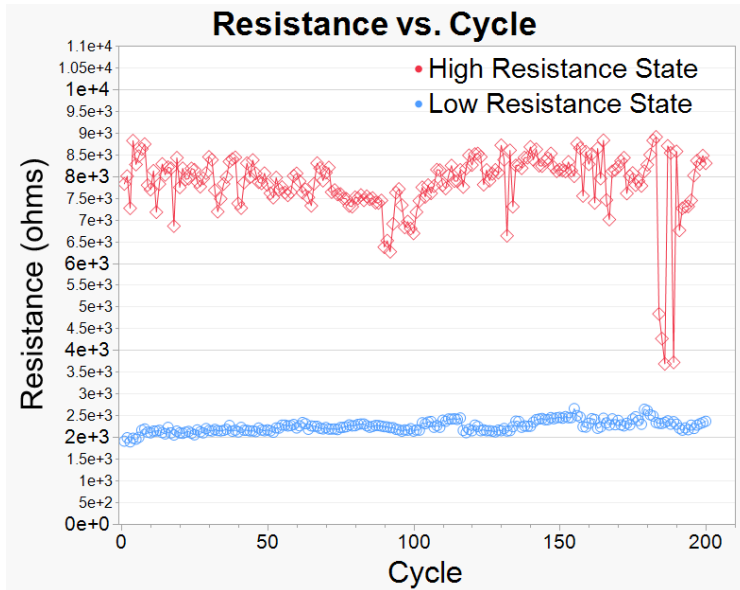
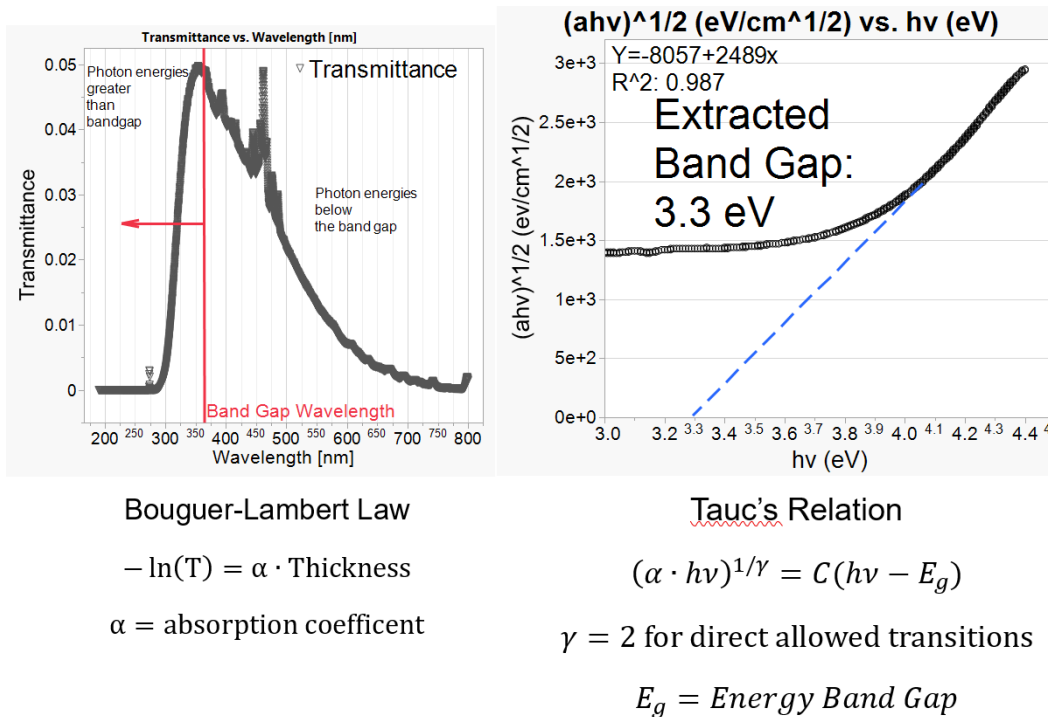


Figure 11: Endurance Test (Resistance vs Cycle)



Bouguer-Lambert Law

$$-\ln(T) = \alpha \cdot \text{Thickness}$$

α = absorption coefficient

Tauc's Relation

$$(\alpha \cdot h\nu)^{1/\gamma} = C(h\nu - E_g)$$

$\gamma = 2$ for direct allowed transitions

$E_g = \text{Energy Band Gap}$

Figure 12: Transmittance versus Wavelength and Tauc Plot used to extract energy band gap.

Relevant equations used to make Tauc Plot shown below.

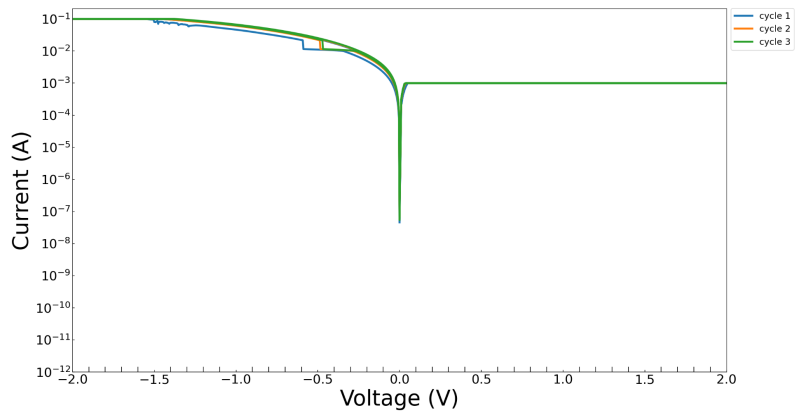


Figure 13: Typical Ni/WO_x/Ni IV Curve