RYERSON UNIVERSITY

Final Report
OFR-RE Project - Future Urban Electric System Project
(Theme 2, Part 2)

Analysis, Design and Implementation of a High Power Fast Charging Station for Plug-in Hybrid Electric Vehicles (PHEVs)

For

Toronto Hydro Electric System Limited (THESL)

and

Centre for Urban Energy (CUE)

Prepared by

S. Rivera, L. Tan, V. Yaramasu, J. Wang and B. Wu

Department of Electrical and Computer Engineering

Ryerson University

Contents

1 Introduction

Level III or fast dc charging is not suitable as an on-board solution, due the power ratings. This is because the higher power capacity will be strongly limited in terms of cost, space and weight in the vehicle [1]. On the other hand, from the grid point of view it also represents a challenge, as the penetration of PEVs increases, the electric system will not be able to provide the demand of power, particularly at peak charging hours. In addition, fast chargers are not suitable for residential use, as a higher power charger is more likely to be a three-phase solution [2]. Besides, the transformers in these areas are not rated to withstand the sudden connection of several fast chargers. For these reasons, the concept of a commercial charging station with installed off-board high power chargers, similar to conventional gas filling stations located at public places (parking lots, work, shopping locations, etc.) appears as a viable solution to enable PEV fast charging.

This charging station could have two possible architectures: featuring the use of an ac bus, where each load is connected to it via independent ac-dc stages; or using a single ac-dc stage to provide a common dc bus for all the loads of the system. The later appears as a more viable solution as the loads are inherently dc, reducing the size and cost of the system and increasing the efficiency due to fewer power conversion stages [3, 4, 5]. Moreover, this structure facilitates the integration of distributed generation or energy storage systems [6].

This report proposes high power conversion stage with a different dc bus concept, using a bipolar dc three-wire distribution system, enabled by a grid-tied three-level neutral point clamped (NPC) converter. This increases the power capacity of the station, as the dc link voltage is doubled. However, the step down effort of the battery chargers is not changed as they are connected to the split dc bus. Due to the fact that the selected topology presents a limited capacity of operation under different dc loads, a voltage balancing circuit is implemented in order to overcome this issue, working only when the system is driven out of the balanced zone, to maximize efficiency. The formal definition of the unbalance limit allows to know a priori the values of the current needed to bring the system back to balance. This enables the use of the bipolar structure under any load scenario while keeping the high quality input currents generated at the ac side and protecting the converter, allowing to feed several high power chargers.

The use of the NPC as the central converter shows several advantages: higher grid power quality (three levels), reduced THD, lower switching frequency, medium voltage operation, lower transformer ratio, etc. [7, 8, 9]. In addition, the power can be scaled up for a larger charging station.

The present report presents a discussion of the selected converter topology, its operation limit and a novel method to overcome it.

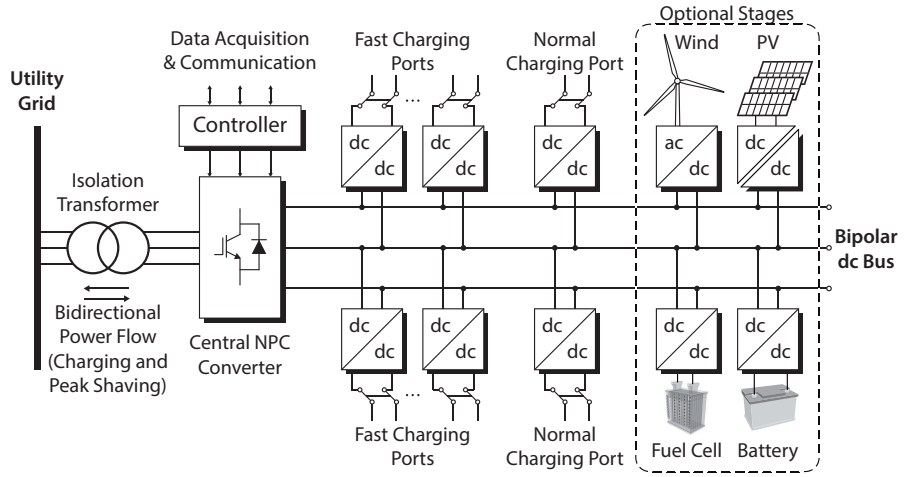


Figure 1: Proposed charging station with bipolar dc bus.

2 Topology Description

2.1 Bipolar dc Bus Architecture

The architecture of the proposed charging station is illustrated in Fig. 1, where a central converter is acting as a single interface with the grid, providing dc power to several charging ports. The charging ports can be either conventional or fast, each one enabled by an independent dc-dc stage. The availability of a distributed dc bus is beneficial for the connection of different distributed power systems such as renewable energy generators (PV or wind) or energy storage devices, like the concept proposed in [6].

The use of a split dc bus offers more flexibility compared to the unipolar dc, as it allows the connection of the loads to two regulated dc voltages: between the neutral connector and either the positive or negative bar; or connecting between the positive and the negative bars [10]. The structure also features higher power capabilities without increasing the switching device ratings or paralleling. Comparing with the unipolar configuration, assuming the same dc voltage for each dc bus and the same input current, the power of the station is doubled. As the bipolar structure is adopted, the balance control becomes essential [11].

Also, this central charging station concept allows several opportunities to provide support to the grid, such as peak power shaving, reactive compensation and power fluctuation minimization. In addition, considering further developments of energy storage devices (batteries and supercaps), will make it possible to provide power back to the grid, enabling Vehicle to Grid (V2G) operation.

2.2 Central Grid-Tied Converter

The topology selected to act as a grid interface is a 4 leg 3-phase NPC converter which is shown in Fig. 2. The addition of an extra leg to the converter is for balancing purposes as it will be

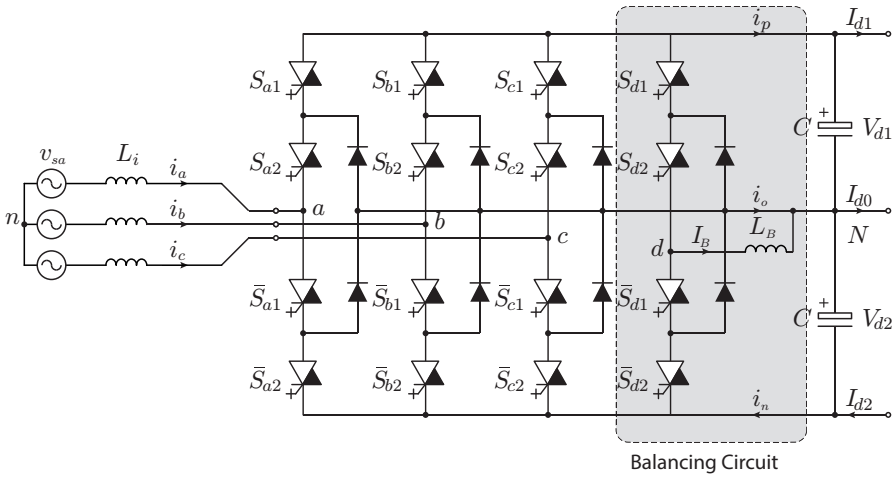


Figure 2: Grid-tied 3-phase NPC converter with a balancing leg.

explained later. This converter offers superior harmonic performance, and also higher power handling capabilities, making possible an extension in the power rating if needed. In addition, if the charger units provide isolation, the need of a bulky and costly isolation transformer at the grid side is not mandatory.

The correct performance of the NPC is only achieved with an accurate control of its mid-point voltage [7]. If the system is used as a unipolar dc bus, the unbalancing problem is not too serious and is usually solved by the modulation stage or by a simple balancing mechanism [8, 12, 13]. However, as the system is providing a bipolar dc bus, and each dc voltage feeds different loads, unbalanced operation is inherent to the system do to the nature of the application. In order to minimize unbalanced condition an alternated connection to the two dc buses can be promoted. Even so, unbalanced operation will occur, and even worst case scenarios in which all loads are connected to one of the two dc buses. Therefore, even if the modulation scheme takes this into consideration, the unbalanced scenarios that the system is able to handle, while keeping the mid-point voltage controlled, is limited[14]. This limitation will be covered in detail in the following sections.

2.3 NPC Unbalanced Bipolar DC Load Limitation

The bipolar dc bus system variables are presented in the NPC topology shown in Fig. 2. The power demanded by the dc load is given by

$$P_d = V_{d1}I_{d1} + V_{d2}I_{d2}. \quad (1)$$

Moreover, to guarantee the correct operation of the NPC, the mid-point voltage must be balanced, then it is assumed for the rest of the analysis that $V_{d1} = V_{d2} = V_d/2$, leading to

$$P_d = \frac{V_d}{2}(I_{d1} + I_{d2}). \quad (2)$$

It is important to note that under balanced operation, $I_{do} \approx 0$. On the other hand, assuming that the power demand at bus 1 (upper)P_{d1} is kept constant, and the power demand at bus 2 (lower) P_{d2} is only a fraction ϵ of it, the previous expression is modified as

$$P_d = \frac{V_d}{2} I_{d1}(1+\epsilon). \tag{3}$$

Note that the polarity of I_{d0} is changed, in order to provide a path for the current excess through the converter neutral point. On the other hand, without loss of generality, it can be assumed that $i_p \approx I_{d1}$, which according to [12], and under unity power factor is given by

$$i_p = \left(\sqrt{3}m_a + \frac{6\alpha}{\pi}\right)\frac{I_s}{2}\cos\delta, \tag{4}$$

where m_a stands for the amplitude modulation index, α is the dc drift of the converter voltage during the positive half cycle (its value is zero under balanced operation), I_s is the amplitude of the input current, and δ is the converter voltage vector angle with respect to the grid voltage. The current i_p is set by the demand in bus 1, therefore does not change under unbalances.

It is important to highlight that (4) shows it is possible to handle some unbalanced scenarios by introducing a dc drift in the generated voltage. However, this value is limited by the linear operation of the modulation stage, suggesting that the balancing capabilities will vary depending on the modulation scheme and the balancing technique, and also it is a function of the amplitude modulation index m_a. Assuming that the system is at its limit, generating the largest dc drift $\hat{\alpha}$ and is able to be brought back to balance. As the power demanded at the lower bus is ϵP_{d1}, the current at the positive bar is given by (see Appendix A for a detailed explanation)

$$i_p = \left(\sqrt{3}m_a + \frac{6\hat{\alpha}}{\pi}\right)\frac{I_s}{2}\frac{1+\epsilon}{2}\cos\delta. \tag{5}$$

However, the demanded current has not changed at the upper bus, thus i_p must still meet (4). Then is possible to solve ϵ using (4) and (5), leading to

$$\epsilon = \frac{2\sqrt{3}m_a}{\sqrt{3}m_a + \frac{6\hat{\alpha}}{\pi}} - 1, \tag{6}$$

where ϵ is the lowest value for the ratio between P_{d1} and P_{d2} that the modulation stage is able to balance. The situation is analogous when the unbalance is in the upper dc bus, due the symmetry of the switching patterns.

The previous analysis states that, if the system is able to operate above the determined value for ϵ, there is no need for another balancing mechanism than the one provided by the modulation stage. However, considering the variable operation of the charging station, it is very unlikely to have a continuous operation within the balancing zone provided by the modulator, therefore an additional balancing technique must be included in order to guarantee the proper operation of the converter in any load scenario.

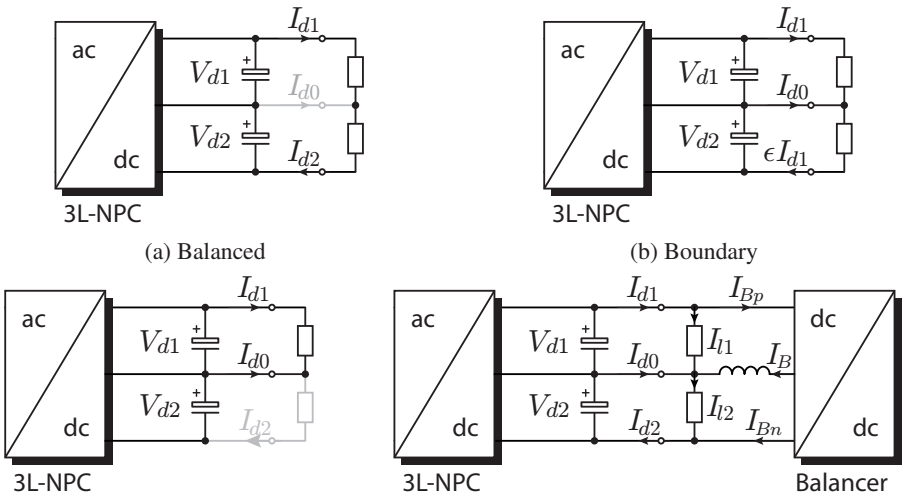
2.4 Voltage Balancing Circuit.

The previous section determines the unbalanced operation limit when operating with different dc loads with the NPC. As for the fast charging station, there is no way to guarantee that the system will never be driven outside the valid operation zone, hence a complimentary balancing mechanism is needed. The operation principle is the following: it is assumed that the modulation scheme allows to operate unbalanced until certain point. Then, to extend the operation range, a virtual impedance will be connected in such a way that, when the system is out of the valid operation zone, it demands the minimum current such as the limit is met.

Considering that in grid connection systems, the modulation index varies slightly and therefore can be assumed to be constant, the minimal load condition in which the balance is achievable is known a priori. It is important to highlight that the polarity of I_{d0} will change depending on whether the load is lighter in the upper dc bus or in the lower dc bus. This means that the balancing circuit must be able to control the current in both directions.

To illustrate the principle of operation, Fig. 3 shows different loads scenarios at the bipolar dc bus system. First, during normal balanced operation of Fig. 6b, both dc loads consume the same power, the current I_{d0} is practically zero, and all the current injected through the positive terminal returns through the negative terminal. During the maximum unbalanced operation shown in Fig. 3b, the power demanded by the lower bus is just a fraction of the upper one, therefore, its current is also a fraction (as the dc voltages are kept balanced), thus only ϵI_{d1} returns through the negative terminal, and the remanent current is conducted through the neutral point, making $I_{d0} = (\epsilon - 1)I_{d1}$. This is the maximum value that the modulation is able to conduct through the neutral point, and any lighter load at the lower dc bus will drive the system out of balance.

Finally, the extreme condition is presented in Fig. 3c where there is no load at the lower bus, it becomes clear that the system cannot be balanced just with the modulation stage, as all



(a) Balanced (b) Boundary

(c) Unbalanced (d) With balancing circuit

Figure 3: Different operating conditions of the charging station.

the current I_{d1} has to be drained through the neutral point. The addition of a balancing circuit, as shown in Fig. 3d, provides a path for the return of the current ϵI_{d1} through the negative bar, keeping the system to operate always at the balanced zone.

This balancing circuit can be implemented in several ways. In [15] a bidirectional boost converter is employed in a five level NPC. For sake of simplicity, this proposal implements a bidirectional boost converter, by using a fourth leg in the NPC, as shown in Fig. 2. Using a leg identical to the other phases of the circuit facilitates design and implementation through PEBB. This is a desirable characteristic in practical applications rather than hybrid converters.

3 Control Scheme

The VOC control scheme is used for the regulation of the converter, as illustrated in Fig. 4. The modulation is performed using the SVM algorithm for a NPC converter [16], and a PI controller has been included to regulate the ponderation for the usage of the negative and positive small vectors, in order to keep the middle point balanced.

For the converter model and control design please refer to the previous reports, as it was already covered, as beside the modulation stage and the mid-point voltage controller the control scheme is basically the same as for a 2L-VSC.

3.1 Neutral Point Voltage Controller

The superior harmonic performance of the selected topology is based on the capability of generating three-level voltage waveforms. However, this capability is dependent on the neutral point voltage of the dc link, therefore it must be accurately controlled. As it can be seen in Fig. 4, this approach uses PI controller to regulate this voltage, and its actuation is fed to the modula-

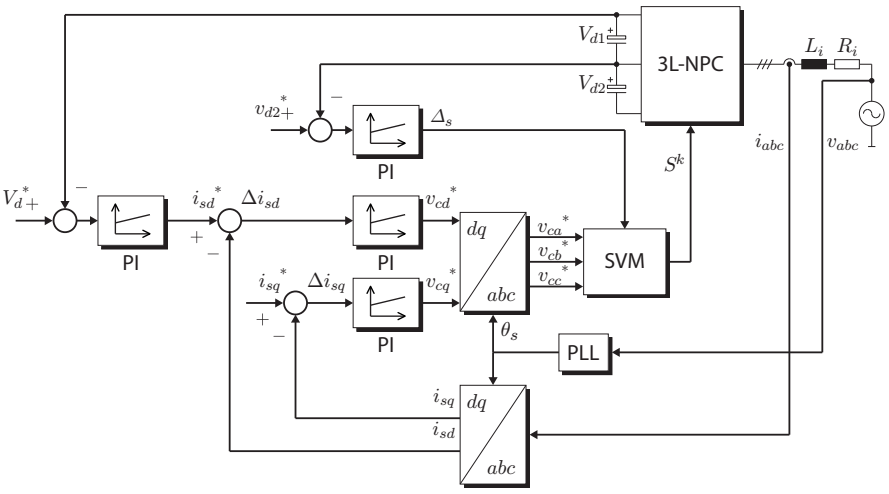


Figure 4: VOC block diagram for the central NPC converter.

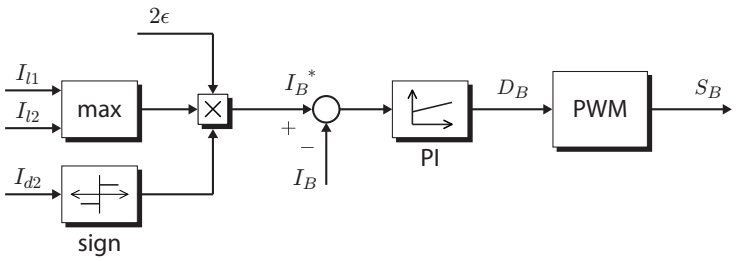


Figure 5: Voltage balancing circuit controller for the additional NPC leg.

tion stage in order to select the proper redundancies and keep the dc voltages balanced. This balancing mechanism will be explained in section 4.

3.2 Voltage Balancing Circuit Control

At this point, the modulation stage provides certain voltage balancing capabilities for the dc buses, and the boundary load is represented by ϵ. In order to extend the balanced operation through the entire load scenario, the voltage balancing circuit must be able to emulate this minimal load condition. Assuming that the value for $\hat{\alpha}$ has been determined, the current reference amplitude is given by (6) and the maximum possible dc drift $\hat{\alpha}$. However, its polarity is still to be determined, to do so, the following analysis is made:

First, the presence of the balancing circuit changes the currents of the system, therefore I_{l1} and I_{l2} will denote the currents circulating through the dc loads at upper and lower buses respectively. Then, if the boundary load is ϵ, and the lower bus has a load outside the valid range, then the additional circuit should demand a current in such a way that, ϵI_{l1} is flowing through the negative bar. This means that I_B is negative. Then, the output current I_{Bn} is related with its input as

$$I_{Bn} = \frac{I_B}{D}. \tag{7}$$

In this case the duty cycle is fixed to 0.5, so the reference current that keeps the system balanced is $I_B^* = -2\epsilon I_{l1}$.

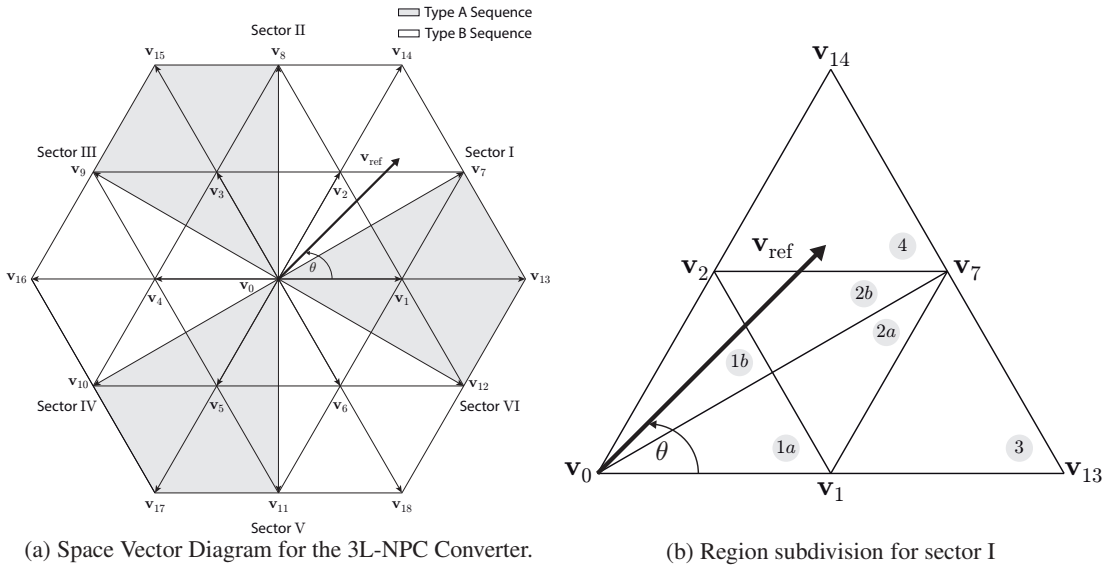
If the unbalance is at the upper bus, then the balancing circuit should demand a current such that ϵI_{l2} is flowing through the positive terminal, making I_B positive. The relation between I_{Bp} and its input is

$$I_{Bp} = \frac{I_B}{1-D}. \tag{8}$$

Thus the reference for the current controller is $I_B^* = 2\epsilon I_{l2}$.

A PI controller is used to regulate the input current of the voltage balancing circuit, as presented in Fig. 5. It should be noted that this control scheme only operates when the system unbalanced in the system is larger than ϵ. Therefore, an enabling signal is defined as follows.

$$e_{\mathrm{B}} = \begin{cases} 1 & \text{if } |I_{l1} - I_{l2}| > (1-\epsilon)\max\{I_{l1}, I_{l2}\} \\ 0 & \text{if } |I_{l1} - I_{l2}| \leq (1-\epsilon)\max\{I_{l1}, I_{l2}\} \end{cases} \tag{9}$$



(a) Space Vector Diagram for the 3L-NPC Converter.

(b) Region subdivision for sector I

Figure 6: SVM Scheme for a 3L-NPC Converter

4 Space Vector Modulation

The space vector modulation (SVM) scheme is a popular real-time digital PWM scheme that offers two degrees of freedom for advanced controller design. In comparison with conventional carrier-based sinusoidal PWM, extends the operation range by a 15% [16]. Considering the discrete nature of the switching devices, and the valid combinations of the gating signals, the converter is able to connect each phase of the load to three voltage levels: $-V_d/2$, 0 and $V_d/2$. This leads to represent the converter voltage vector $\mathbf{v}_c$ as a function of the phase switching state $S = (S_a, S_b, S_c)$ and the dc link voltage V_d as

$$\mathbf{v}_c = \frac{V_d}{3}(S_a + \mathbf{a}S_b + \mathbf{a}^2 S_c), \text{ where } S_k \in \{\text{N,O,P}\}, \text{ and } k = a, b, c. \tag{10}$$

This means that the converter is able to generate 19 different voltage vectors (out of 27 different valid switching states), as it can be seen in Fig. 9a. It is possible to see that there are six small active vectors $\mathbf{v}_1$ to $\mathbf{v}_6$ (each one has a positive and negative redundancy), six medium vectors $\mathbf{v}_7$ $\mathbf{v}_{12}$, six large vectors $\mathbf{v}_{13}$ to $\mathbf{v}_{18}$, and the zero vector $\mathbf{v}_0$ (which has three redundancies). Table 1 resumes the switching states for each available vector. The Space Vector Modulation (SVM) technique takes into account the available vectors of the system and provides an output with variable amplitude and variable frequency, whose are defined by the rotating reference vector $\mathbf{v}_{\text{ref}}$. The operating principle is based on a discrete time control platform with a fixed sampling time T_s. During this sampling time $\mathbf{v}_{\text{ref}}$ can be considered constant and it can be synthesized using the three closest vectors (two of them active and the other one zero), by applying them for a certain period of time, called dwell times, which essentially represent the duty cycle for the switches which generates these vectors.

In order to identify the closest stationary vectors, the $\alpha - \beta$ stationary plane must be discretized into six sectors, as presented in Fig. 6a. To make this discretization, the angle of the reference vector θ must be obtained. This angle is defined as

$$\theta \quad = \quad \arctan\left(\frac{v_\beta}{v_\alpha}\right), \tag{11}$$

where v_α and v_β represent the real and imaginary parts of $\mathbf{v}_{\text{ref}}$ respectively. After obtaining θ, the discretization of the plane is defined as follows

$$(k-1)\frac{\pi}{3} \leq \theta_k < k\frac{\pi}{3}, \tag{12}$$

where θ_k stands for the k-th sector. As a difference with the conventional SVM scheme for the 2L-VSC, the sectors have to be subdivided into 6 regions as it is shown in Fig. 6b, due the larger vector availability of the NPC.

Therefore, using the sector information given by θ_k along with the proper detection of the region, the dwell times can be calculated. Using the example case provided in Fig. 6b, is possible to see that the $\mathbf{v}_{\text{ref}}$ is located in sector I region 4 (or region I-4 for the rest of the report). Then, this voltage can be synthesized as

$$\mathbf{v}_{\text{ref}} \quad = \quad \frac{1}{T_s}(t_a\mathbf{v}_2 + t_b\mathbf{v}_7 + t_c\mathbf{v}_{14}). \tag{13}$$

Separating (13) into its real and imaginary parts, and using the stationary vector information provided by Table 1 leads to

Table 1: 3L-NPC Space Vectors

Vector	Switching State	Output Voltage	Vector	Switching State	Output Voltage
$\mathbf{v}_0$	[NNN][OOO][PPP]	0			
$\mathbf{v}_{1\text{P}}$	[POO]	$\frac{V_d}{3}$	$\mathbf{v}_7$	[PON]	$\frac{V_d}{\sqrt{3}}e^{j\frac{\pi}{6}}$
$\mathbf{v}_{1\text{N}}$	[ONN]		$\mathbf{v}_8$	[OPN]	$\frac{V_d}{\sqrt{3}}e^{j\frac{\pi}{2}}$
$\mathbf{v}_{2\text{P}}$	[PPO]	$\frac{V_d}{3}e^{j\frac{\pi}{3}}$	$\mathbf{v}_9$	[NPO]	$\frac{V_d}{\sqrt{3}}e^{j\frac{5\pi}{6}}$
$\mathbf{v}_{2\text{N}}$	[OON]		$\mathbf{v}_{10}$	[NOP]	$\frac{V_d}{\sqrt{3}}e^{j\frac{7\pi}{6}}$
$\mathbf{v}_{3\text{P}}$	[OPO]	$\frac{V_d}{3}e^{j\frac{2\pi}{3}}$	$\mathbf{v}_{11}$	[ONP]	$\frac{V_d}{\sqrt{3}}e^{j\frac{3\pi}{2}}$
$\mathbf{v}_{3\text{N}}$	[NON]		$\mathbf{v}_{12}$	[PNO]	$\frac{V_d}{\sqrt{3}}e^{j\frac{11\pi}{6}}$
$\mathbf{v}_{4\text{P}}$	[OPP]	$\frac{V_d}{3}e^{j\pi}$	$\mathbf{v}_{13}$	[PNN]	$\frac{2V_d}{3}$
$\mathbf{v}_{4\text{N}}$	[NOO]		$\mathbf{v}_{14}$	[PPN]	$\frac{2V_d}{3}e^{j\frac{\pi}{3}}$
$\mathbf{v}_{5\text{P}}$	[OOP]	$\frac{V_d}{3}e^{j\frac{4\pi}{3}}$	$\mathbf{v}_{15}$	[NPN]	$\frac{2V_d}{3}e^{j\frac{2\pi}{3}}$
$\mathbf{v}_{5\text{N}}$	[NNO]		$\mathbf{v}_{16}$	[NPP]	$\frac{2V_d}{3}e^{j\pi}$
$\mathbf{v}_{6\text{P}}$	[POP]	$\frac{V_d}{3}e^{j\frac{5\pi}{3}}$	$\mathbf{v}_{17}$	[NNP]	$\frac{2V_d}{3}e^{j\frac{4\pi}{3}}$
$\mathbf{v}_{6\text{N}}$	[ONO]		$\mathbf{v}_{18}$	[PNP]	$\frac{2V_d}{3}e^{j\frac{5\pi}{3}}$

$$v_{\text{ref}} \cos\theta = \frac{1}{T_s}\left(\frac{1}{6}t_a V_d + \frac{1}{2}t_b V_d + \frac{1}{3}t_c V_d\right) \tag{14}$$

$$v_{\text{ref}} \sin\theta = \frac{1}{T_s}\left(\frac{\sqrt{3}}{6}t_a V_d + \frac{\sqrt{3}}{6}t_b V_d + \frac{\sqrt{3}}{3}t_c V_d\right). \tag{15}$$

On the other hand, the dwell times must comply with

$$T_s = t_a + t_b + t_c. \tag{16}$$

Then, isolating t_a, t_b and t_c, and introducing the modulation index $m_a = \sqrt{3}v_{\text{ref}}/V_d$, the dwell times for the example are given by

$$t_a = 2T_s - 2T_s m_a \sin\left(\theta + \frac{\pi}{3}\right) \tag{17}$$

$$t_b = 2T_s m_a \sin\left(\frac{\pi}{3} - \theta\right) \tag{18}$$

$$t_c = 2T_s m_a \sin\theta - T_s. \tag{19}$$

Extending the same idea for the entire stationary plane and considering the seven-segment sequence provided in [16] the Tables 2 and 3 are obtained for the calculation of the dwell times.

4.1 SVM Unbalanced Operation Limit

In order to control the mid-point voltage in the NPC, the small vectors usage is redistributed to bring the system back to balance. In this way the tracking of the reference is not altered. To illustrate the principle, revisit the example shown in Fig. **??**, the reference vector can be synthesized according to (13)

Table 2: Dwell times calculation 3L-SVM for odd sectors

Region	t_a	t_b	t_c
$1a$	$2m_a \sin(\theta_1 - \theta)$	$2m_a \sin(\theta - \theta_2)$	$1 - 2m_a \sin(\theta - \theta_3)$
$1b$	$2m_a \sin(\theta - \theta_2)$	$1 - 2m_a \sin(\theta - \theta_3)$	$2m_a \sin(\theta_1 - \theta)$
$2a$	$1 - 2m_a \sin(\theta - \theta_2)$	$1 - 2m_a \sin(\theta_1 - \theta)$	$2m_a \sin(\theta - \theta_3) - 1$
$2b$	$1 - 2m_a \sin(\theta_1 - \theta)$	$2m_a \sin(\theta - \theta_3) - 1$	$1 - 2m_a \sin(\theta - \theta_2)$
3	$2 - 2m_a \sin(\theta - \theta_3)$	$2m_a \sin(\theta_1 - \theta) - 1$	$2m_a \sin(\theta - \theta_2)$
4	$2 - 2m_a \sin(\theta - \theta_3)$	$2m_a \sin(\theta_1 - \theta)$	$2m_a \sin(\theta - \theta_2) - 1$

where $\theta_1 = \frac{k\pi}{3}$, $\theta_2 = \frac{(k-1)\pi}{3}$, $\theta_3 = \frac{(k-2)\pi}{3}$ and k stands for the sector number.

Table 3: Dwell times calculation 3L-SVM for even sectors

Region	t_a	t_b	t_c
$1a$	$2m_a \sin(\theta_1 - \theta)$	$1 - 2m_a \sin(\theta - \theta_3)$	$2m_a \sin(\theta - \theta_2)$
$1b$	$2m_a \sin(\theta - \theta_2)$	$2m_a \sin(\theta_1 - \theta)$	$1 - 2m_a \sin(\theta - \theta_3)$
$2a$	$1 - 2m_a \sin(\theta - \theta_2)$	$2m_a \sin(\theta - \theta_3) - 1$	$1 - 2m_a \sin(\theta_1 - \theta)$
$2b$	$1 - 2m_a \sin(\theta_1 - \theta)$	$1 - 2m_a \sin(\theta - \theta_2)$	$2m_a \sin(\theta - \theta_3) - 1$
3	$2 - 2m_a \sin(\theta - \theta_3)$	$2m_a \sin(\theta - \theta_2)$	$2m_a \sin(\theta_1 - \theta) - 1$
4	$2 - 2m_a \sin(\theta - \theta_3)$	$2m_a \sin(\theta - \theta_2) - 1$	$2m_a \sin(\theta_1 - \theta)$

where $\theta_1 = \frac{k\pi}{3}$, $\theta_2 = \frac{(k-1)\pi}{3}$, $\theta_3 = \frac{(k-2)\pi}{3}$ and k stands for the sector number.

To determine the maximum injected dc drift $\hat{\alpha}$, the average usage time for the small vectors t_a is calculated over the positive half cycle (see Appendix A). During normal operation and using the example, t_a is equally divided in the redundancies of $\mathbf{v}_2$, $\mathbf{v}_{2\mathrm{N}}$ and $\mathbf{v}_{2\mathrm{P}}$, thus the maximum available time to redistribute is $t_a/2$. This remaining time is equivalent to the maximum dc drift that can be injected before leaving the linear zone of the modulation, and varies with m_a, as the reference will pass through different regions of the sector depending on its value. In order to calculate this time, the average value dwell-times from Table 2 and Table 3 for each small vector are obtained during its corresponding interval. The resulting average expression for the maximum voltage drift is defined in (20), where θ is the angle at which the change of region occurs.

$$\hat{\alpha} = \begin{cases} \frac{-3m_a + 6m_a \sin\left(\theta + \frac{\pi}{6}\right)}{\pi}, & \theta = \frac{\pi}{6}, & \text{if } 0 \leq m_a < \frac{1}{2} \\ \frac{\frac{\pi}{2} + 3m_a - 3\theta - 6m_a \cos(\theta) + 6m_a \sin\left(\theta + \frac{\pi}{6}\right) + 3m_a\sqrt{3}}{\pi}, & \theta = \arcsin\left(\frac{1}{2m_a}\right) - \frac{\pi}{3}, & \text{if } \frac{1}{2} \leq m_a < \frac{1}{\sqrt{3}} \\ \frac{\frac{\pi}{2} - 3m_a + 3\theta - 6m_a \cos(\theta) + 6m_a \cos\left(\theta + \frac{\pi}{3}\right) + 3m_a\sqrt{3}}{\pi}, & \theta = \frac{\pi}{3} - \arcsin\left(\frac{1}{2m_a}\right), & \text{if } \frac{1}{\sqrt{3}} \leq m_a < 1 \end{cases} \quad (20)$$

As it was mentioned earlier, a PI linear controller is used to keep the mid-point voltage at its reference, as presented in Fig. 4. Its actuation Δ_s is used to modify the positive and negative small vectors dwell-times t_{a_P} and t_{a_N} as:

$$t_{a_P} = \frac{t_a}{2}(1 - \Delta_s), t_{a_N} = \frac{t_a}{2}(1 + \Delta_s). \quad (21)$$

Note that this is in the case that the load is demanding current from the grid. In the case of having active loads, the sign of Δ_s must be modified accordingly to be able to balance the system as the effect of the small vectors is reversed.

Considering the balancing strategy, and the maximum value of α achieved under this modulation scheme, Fig. 7 shows the theoretical unbalanced operation limit of the NPC providing a

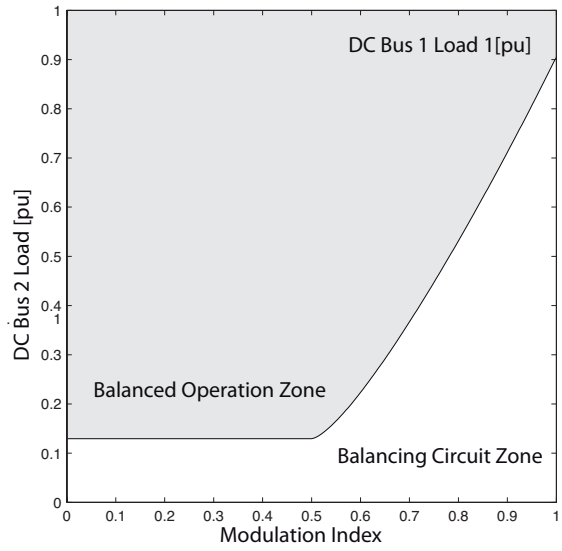


Figure 7: Load unbalance limitation for the NPC using SVM.

bipolar dc bus, when the balancing is made by redistributing the usage of the small vectors. Is important to mention that the balancing circuits operates when the system is driven outside the gray area of balanced operation.

4.2 Switching Sequence

The dwell times have already been determined to synthesize the voltage reference. However, a proper sequence of the vectors must be defined, which will vary depending on the application requirements as reduced switching frequency, symmetrical voltage generation, dc balancing capabilities, etc. In this work the switching sequence used is based in the seven level segment

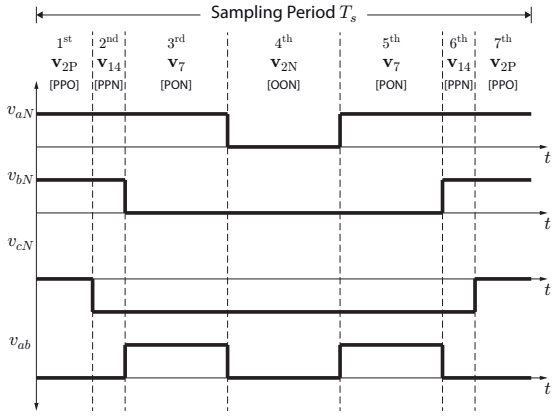
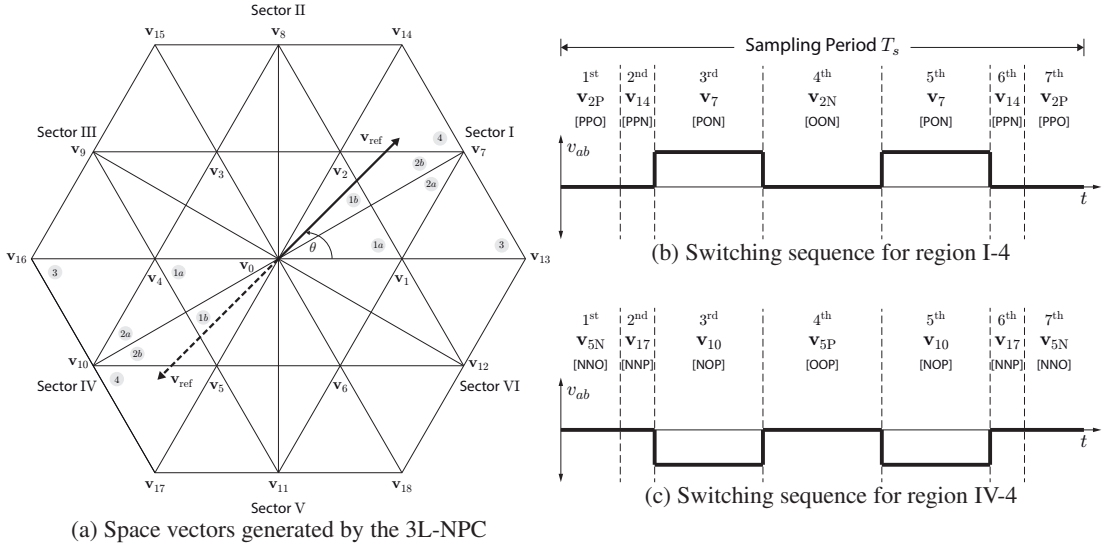


Figure 8: Seven segment switching sequence for SVM.



(a) Space vectors generated by the 3L-NPC

(b) Switching sequence for region I-4

(c) Switching sequence for region IV-4

Figure 9: SVM Operating principle for regions I-4 and IV-4.

proposed in [17]. This method basically consists in dividing one sampling time T_s in seven segments as shown in Fig. 8 and perform transitions which involve only two switches at a time, resulting in a reduced switching frequency on the devices. In addition the method alternates type A (sequence which starts with a negative small vector) and type B (starts with a positive small vector) sequences for the regions that lie 180 apart from each other, in order to achieve half-wave symmetry. This characteristic results in signals free of even order harmonics, an attractive feature for grid connected operation.

To illustrate the principle Fig. 9a shows a suggested case to be analyzed. It can be seen that the reference vector $\mathbf{v}_{\text{ref}}$ is in region I-4 and then IV-4 (which are 180 apart). The sequences needed to synthesize the reference vector are respectively

$$\mathbf{v}_{\text{ref}} = f_s(t_a\mathbf{v}_2 + t_b\mathbf{v}_7 + t_c\mathbf{v}_{14}) \quad (22)$$

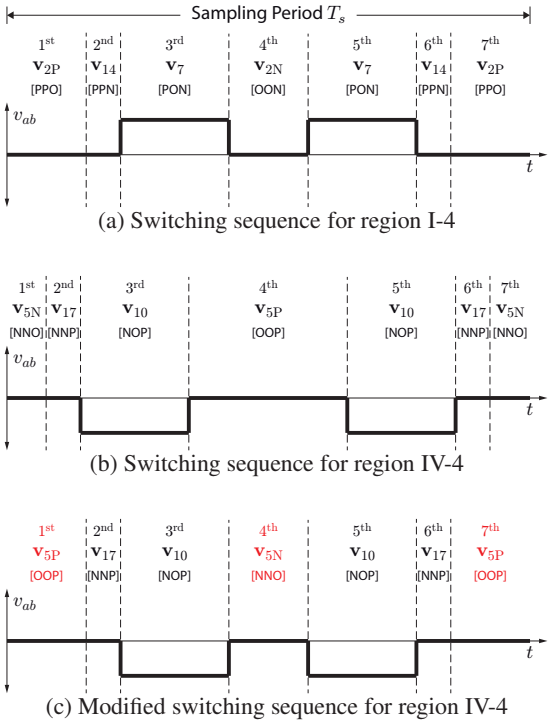
$$\mathbf{v}_{\text{ref}} = f_s(t_a\mathbf{v}_5 + t_b\mathbf{v}_{10} + t_c\mathbf{v}_{17}), \quad (23)$$

where f_s is the sampling frequency of the controller.

The switching sequence needed and the resulting line-to-line voltages are shown in Fig. 9. It can be seen that the sequence used for region I-4 is type A, while for region IV-4 is type B, and the resulting line-to-line voltage waveform has half-wave symmetry.

4.2.1 Unbalanced Scenario Sequence

Considering the results obtained in [18], the main drawback of the control scheme was the presence of even order harmonics in the line current during the unbalanced load operation, because the half-wave symmetry was missed. This is not desirable for grid-connected tasks as the grid code sets stringent limits for this particular components, thus it has to be solved. Therefore the



(a) Switching sequence for region I-4

(b) Switching sequence for region IV-4

(c) Modified switching sequence for region IV-4

Figure 10: Switching sequences for the unbalanced case.

SVM switching sequence will be modified during this instants in order to retrieve the half-wave symmetry and guarantee line currents without even order harmonics.

As mentioned earlier, the dwell-times for positive and negative small vectors are redistributed accordingly, using a PI controller to maintain the dc voltages balanced. To do so, the controller actuation Δ_s is fed to the SVM modulatior to adjust the dwell-times according to (21).

Considering the same voltage reference of the analyzed scenario, but a unbalance at the dc side that results in $\Delta_s = -1/3$, leads to $t_{a_P} = 2t_{a_N}$. The resulting sequences are shown in Fig. 10. It becomes clear that the balancing mechanism has modified the switching sequence, leading to a lack of half-wave symmetry on the line to line voltages. This yields to the appearance of even-order harmonics on the line currents.

As the dwell-times redistribution is needed to achieve balance on the dc voltages, a modification on the switching sequence is proposed, to be used only when the dc loads are different. This modification is simply to swap the position of the negative and positive vectors in one of the the sequences, in order to retrieve the half wave symmetry. In the proposed example, the type B sequence is modified by swapping $\mathbf{v}_{5P}$ and $\mathbf{v}_{5N}$. Is important to note that the condition of changing only two switches per segment is missed due the swapping of the small vectors. This leads to the switching sequence presented in Fig. 10c for the region IV-4.

Table 4: Simulation Parameters

Paramenter	Symbol	Value
Grid Voltage Amplitude	V_s	1 pu
Grid Frequency	f_s	1 pu
Input Filter Inductance	L_i	0.1 pu
Input Filter Resistance	R_i	0.02 pu
dc Link Capacitance	C	2 pu
dc Link Voltage	V_d	2.174 pu
Boost inductance	L_B	0.72 pu
Switching Frequency	f_{sw}	36 pu
Modulation Index	m	0.6408
Load Ratio Limit	ϵ	0.2788
Base Voltage	V_{B}	208 V
Base Power	P_{B}	20 kW
Base Frequency	f_{B}	60 Hz

5 Simulation Results

To validate the proposed architecture a 20 kW 4-phase NPC based charging station system has been simulated using Matlab/Simulink®. The SVM algorithm is programmed in order to have an equivalent switching frequency on the devices of 1080 Hz. The simulation parameters are presented in Table 4.

In order to evaluate the performance of the voltage balancing logic the following dynamic test is performed: the system is operating at rated condition in both dc buses (balanced condition), then at $t = 0.1$ s the load connected at dc bus 1 is removed, while dc bus 2 is kept loaded at rated condition. At $t = 0.2$ s another load impact is performed, a rated load is connected back to dc bus 1 and at the same time the load is disconnected from dc bus 2. Finally at $t = 0.3$ s both buses go back to the rated load condition.

Before discussing the dynamic response of the system, steady state waveforms and harmonic content of the converter voltage v_{aN} are presented in Fig. 11 for the simulated scenarios, to illustrate the balancing mechanism. As it could be expected, during balanced operation, there is no dc drift injected into the converter voltage, therefore, the pulse widths are symmetrical during the positive and negative half cycles, as it can be observed in Fig. 11a. Then, when the upper dc bus has a lighter load, the balancing mechanism imposes a negative dc drift, making the pulses in the negative half cycle wider, like in Fig. 11b. The opposite effect is observed in Fig. 11c, where the dc drift is positive as it can be seen in the wider pulses during the positive half cycle. It can also be noted how the modification of the switching sequence leads to additional commutations on the devices, as it was expected. The dc drift becomes obvious by analyzing the voltage

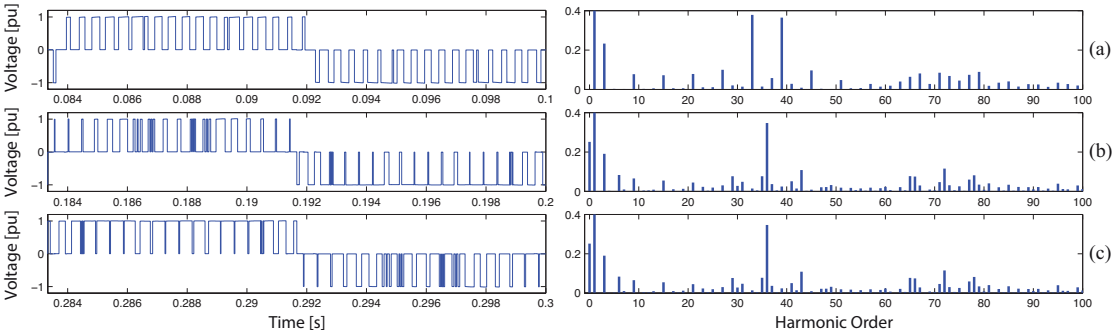


Figure 11: Steady state waveform and harmonic content of the converter voltage v_{aN}: a) Balanced operation; b) No load at dc Bus 1; c) No load at dc Bus 2.

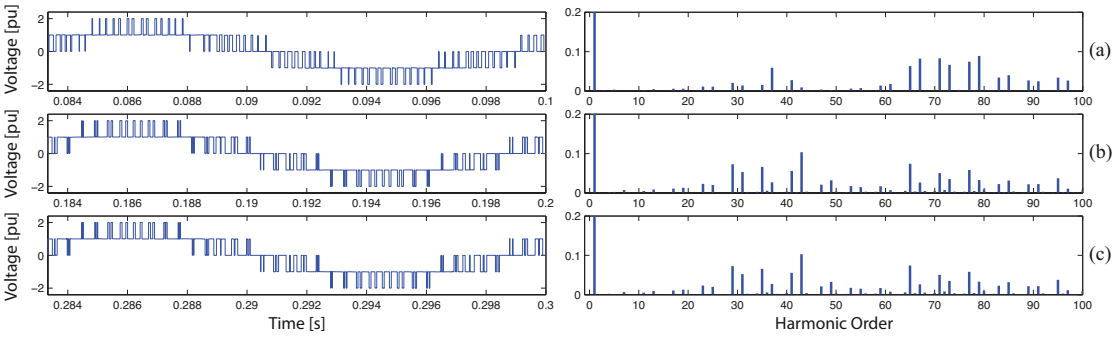


Figure 12: Steady state waveform and harmonic content of the converter line-to-line voltage v_{ab}: a) Balanced operation; b) No load at dc bus 1; c) No load at dc bus 2.

spectrums. It should be noted that because of the balancing method, the half wave symmetry is missed and even order harmonics appear in the unbalanced scenarios of Figures 11b and 11c.

On the other hand, the controller modifies the three phases of the converter equally, therefore the dc drift is not reflected to the line-to-line voltages nor the input currents. This can be confirmed by Fig. 12, showing the waveform of the line-to-line voltage during the three scenarios. It can be seen that their mean value remains to be zero. For the unbalanced cases, these voltages now achieve half-wave symmetry due the modification in the switching sequence during the unbalanced operation, detail which is confirmed by their harmonic content presented in Fig. 12, showing that the cancellation of the even and triplen harmonics remains under the presence of unbalanced loads, as shown in Figures 12b and 12c. Is important to mention that the adjustment performed does not have any impact on the THD of the line currents as it only redistributes the energy concentrated on the harmonic components.

To complete the analysis, the dynamic performance of the system is presented in Fig. 13. First, to illustrate the operation principle of the balancing circuit, the dc currents are presented in Fig. 13a. Before $t = 0.1$ s the system is balanced, therefore I_{l1} and I_{l2} are at rated condition,

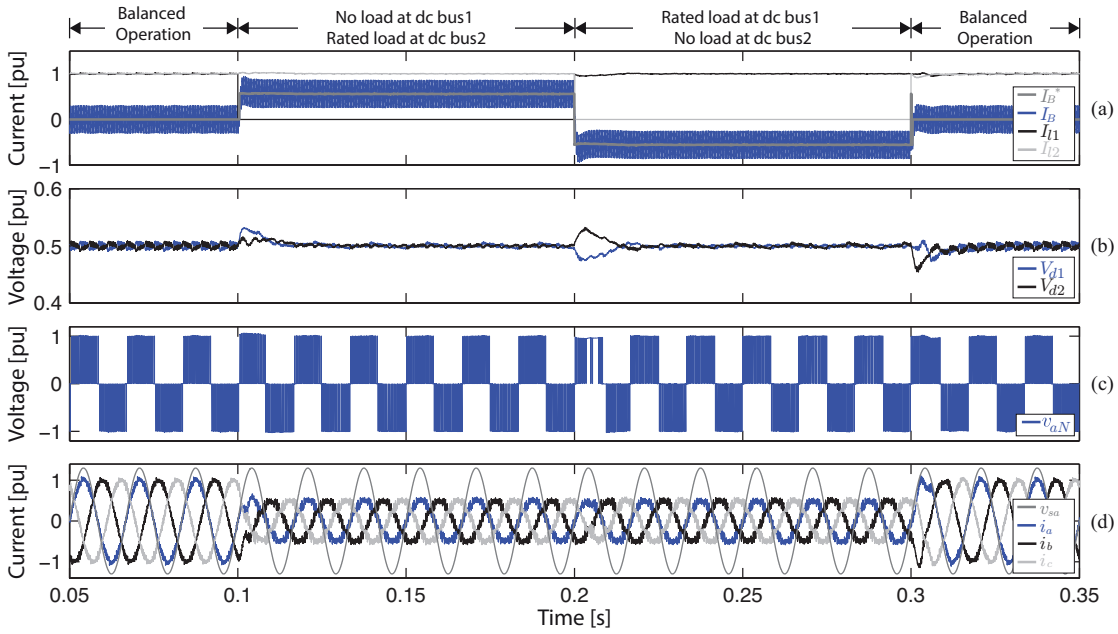


Figure 13: Simulated dynamic response of the system: a) dc currents; b) dc bus voltages; c) converter voltage v_{aN}; d) grid currents.

therefore there is no need to use the balancing circuit. Therefore, the boost current I_B and its reference are kept at zero. Then after the first impact, I_{l1} goes to zero, and I_B is quickly set to $2\epsilon I_{l2}$, while I_{l2} is not affected.

When the second load impact is performed at $t = 0.2$ s, the direction of I_B is changed in order to bring the system back to balance, and its amplitude is $2\epsilon I_{l1}$. As there is no load connected to bus 2, I_{l2} is zero. To conclude, after $t = 0.3$ s, the system is again operated at rated condition, making the balancing circuit not to operate and the boost current is set to zero.

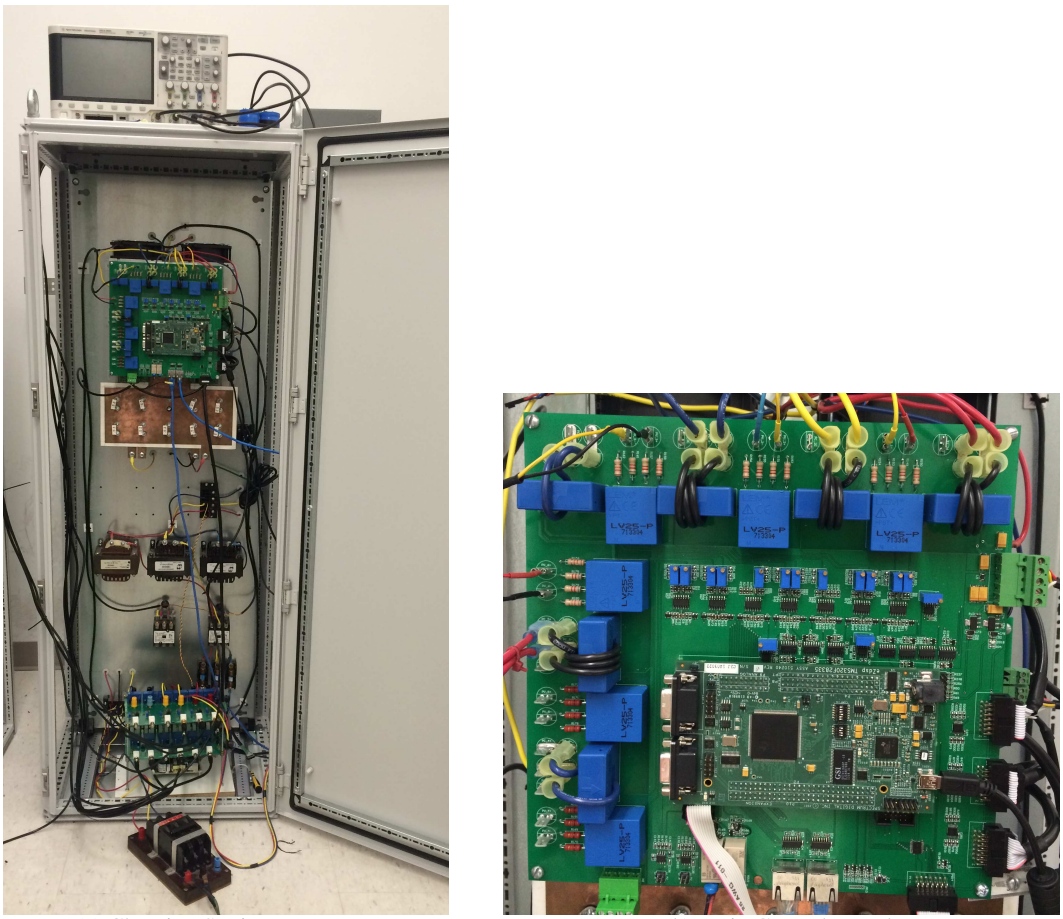
Note that the dc voltages are controlled and kept balanced during the entire operation of the system, illustrated in Fig. 13b. This condition can be corroborated by the waveform of the converter voltage v_{aN} in Fig. 13c, which exhibits similar $\mathrm{d}v/\mathrm{d}t$s during the positive and negative half cycles.

Finally, the previous conditions lead to the input currents shown in Fig. 13d. It can be seen that during the load impacts, do not experience too much distortion, and after a short transient they remain highly sinusoidal and in phase with the grid voltage, thus operating with unity power factor. Despite the reduced switching frequency of the devices, the current presents a THD of 4.71%, which is within the limit imposed by the grid code [19].

6 Experimental Results

In order to complete the validation for the proposed architecture, experimental results are obtained using a 10 kW four leg three-phase NPC based charging station prototype, shown in Fig. 14a. Both balancing approaches will be applied to illustrate their effectiveness and also highlighting its features and drawbacks.

As it can be seen, the setup consists of an inductive filter, an IGBT based four leg NPC converter, and a resistive load connected to each dc bus using a relay unit. The control platform used is a eZdsp (TMS320F28335) from Spectrum Digital, which is performing the main calculations and control actions, along with a Altera Cyclone FPGA to perform peripherials and protections. The control platform is shown in Fig. 14b. Using the parameters presented in Table 4 the control scheme is applied to the converter. In order to confirm the performance of the voltage balancing under any scenario, a dynamic test is performed similar to the simulation study given in the previous section.



(a) Charging Station Prototype

(b) Main Control Board

Figure 14: Photographs of the experimental setup.

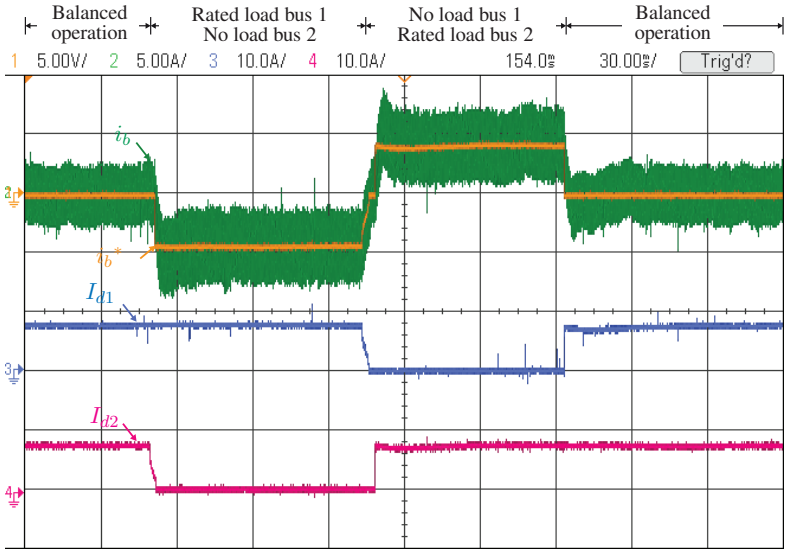


Figure 15: Experimental dynamic performance of the system with method 1. Ch1 boost current reference i_b^* (5 V/div). Ch2 boost current i_b (5 A/div). Ch3 bus 1 load current I_{d1} (10 A/div). Ch4 bus 2 load current I_{d2} (10 A/div). Time scale 30 ms/div.

6.0.2 Dynamic Response

The dynamic performance of the charging station is presented in Figures 15 and 16. It can be seen that the overall behavior of the system is very close to the simulation results.

The dc currents are presented in Fig. 15. The control algorithm is able to extend the balanced operation of the NPC by adjusting the system currents through the bidirectional boost. As it was shown in the previous section, the boost generates a negative current to compensate the no load condition on the lower bus, and positive for the no load condition on the upper bus. It can be seen that the response of the controller allows reaching steady-state within two fundamental cycles. The main difference with the simulation results is the response of the relay, as it exhibits a small delay in the disconnection of the loads.

The evolution of the main controlled variables in the VOC loop is presented in Fig. 16, it can be seen that the system is able to maintain the balance on the dc voltages during the whole test, presenting minimal deviations from its reference in the transient periods. Additionally, it is confirmed that in steady-state, the voltages V_{d1} and V_{d2} are perfectly balanced. This balance at the dc side allows to have a high input current quality, as it can be seen in the evolution of i_{ga}. This current is kept highly sinusoidal during the rated load condition, while during the unbalanced operation its quality decreases accordingly with the reduction on the fundamental amplitude. Moreover, it can be seen that the system operates with unity power factor during the whole test, as the grid current is kept in phase with the grid voltage.

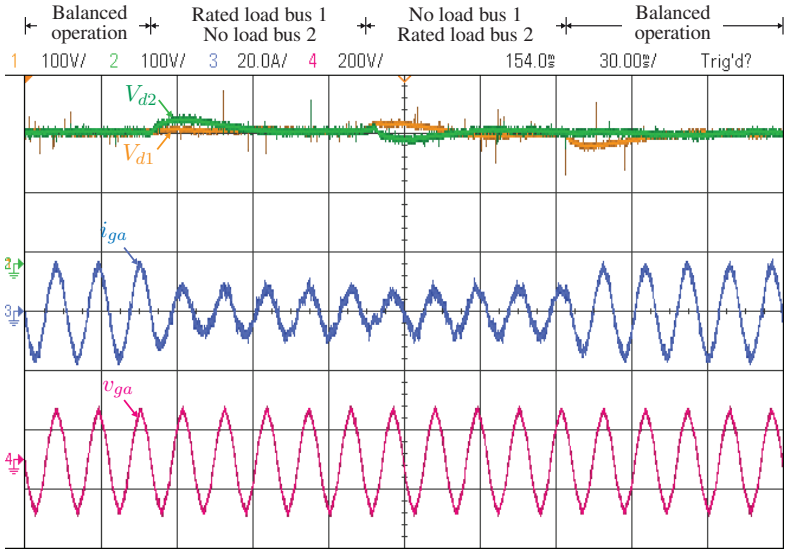


Figure 16: Experimental dynamic performance of the system with method 1. Ch1 dc bus 1 voltage V_{d1} (100 V/div). Ch2 dc bus 2 voltage V_{d2} (100 V/div). Ch3 grid current i_{ga} (20 A/div). Ch4 grid voltage v_{ga}(200 V/div). Time scale 30 ms/div.

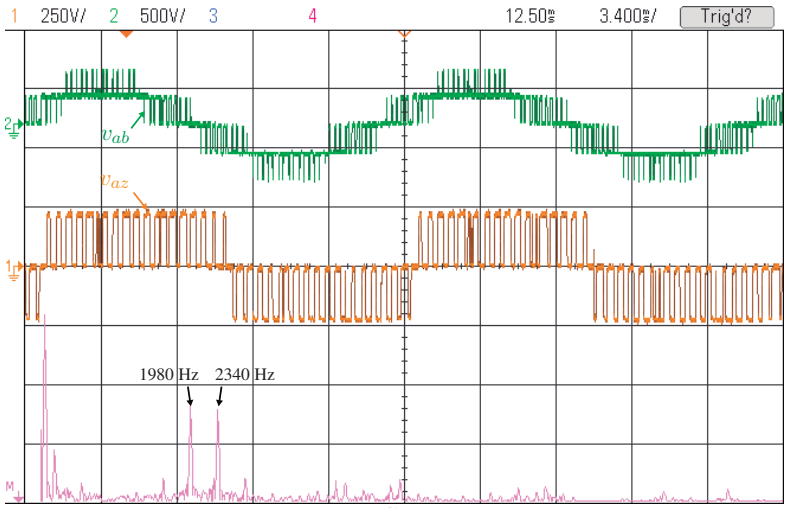
6.0.3 Steady-state Analysis

The waveforms for the voltages generated by the converter are presented in Figure 17, showing both, the phase to neutral v_{az} and the line-to-line v_{ab} during steady-state operation. During the balanced operation, it is clear that no dc bias is been injected to v_{az}, as there is no current flowing through the converter neutral point. The waveform presents half wave symmetry, leading to a harmonic content free of even order harmonics. The spectrum provided shows that the dominant harmonics are located in the sidebands around the component m_f. The resulting waveform for v_{ab} presents a steeped waveform with five levels, clearly defined due to the proper regulation of the mid-point voltage.

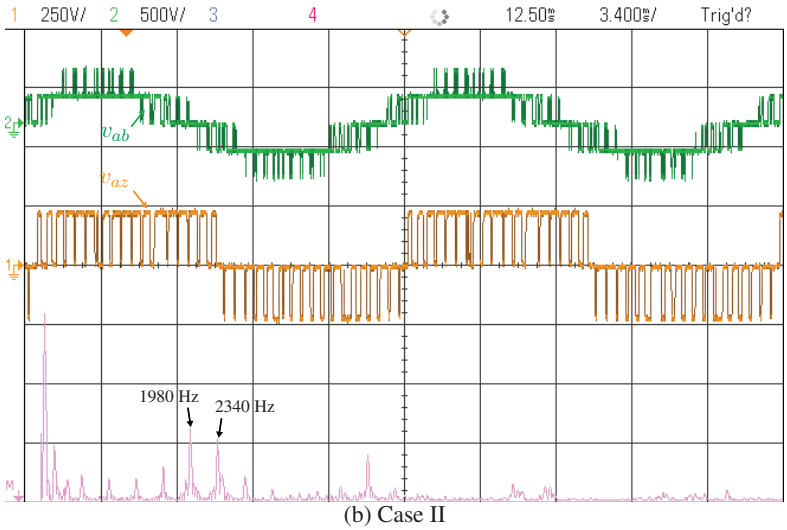
The dc drift injected by the mid-point controller becomes obvious in Fig. 17b. In case II, the system is compensating the no load condition in the lower bus by injecting a positive dc value, making the pulses wider in the positive half cycle. Because of this, the symmetry in the generated voltage is missed, leading to the appearance of even order components in its spectrum, which will have an impact on the demanded current distortion. Nevertheless, as the compensation is injected equally to the three phases of the converter, the line-to-line voltages present a zero dc value in all the scenarios. It is interesting to note that the dominant harmonics of the current have shifted to lower frequencies, situation which can be explained by the loss of half-wave symmetry.

To complete the analysis in steady-state the ac side quantities are illustrated in Fig. 18. The experimental waveforms for the rated load condition of case I are presented in Fig. 18a. The results obtained confirm the correct performance of the proposed control scheme. The accuracy on the control of the mid point-voltage becomes clear, as the dc buses voltages are kept

balanced, leading to high quality currents at the input side. The current i_{ga} exhibits a highly sinusoidal behavior, with a fundamental of 15.35 A, reduced ripple and is in phase with v_{ga}, resulting in a THD of 5.8% for the rated load condition. It also becomes evident the harmonic distortion present in the grid voltage. Then, in the unbalanced operation case of Fig. 18b, it can be seen that the system is able to operate properly even if one of the loads is disconnected at the dc side. The current is kept sinusoidal, but its ripple has increased, this is explained by the reduction of fundamental component of the current to 7.58 A, and as it was established earlier, the modulation index in grid tied operation with unity power factor varies slightly under differ-

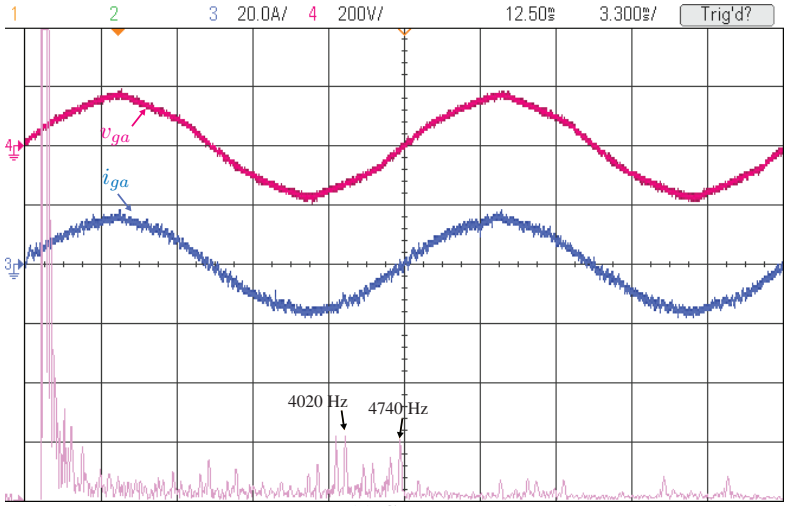


(a) Case I

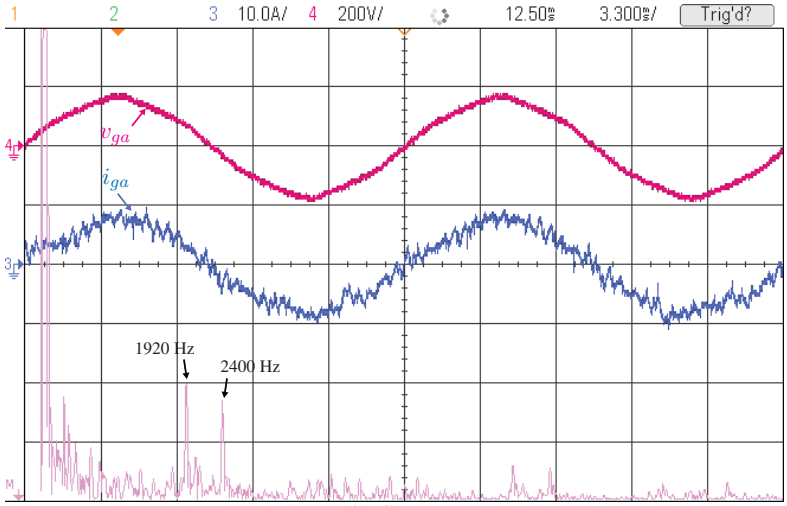


(b) Case II

Figure 17: Experimental converter voltages with method 1. Ch1 phase voltage v_{az} (250 V/div). Ch2 line-to-line voltage v_{ab} (500 V/div). ChM FFT for v_{az} (20 V/div, Span 10 kHz, Center 4.8 kHz). (a) Case I, balanced operation. (b) Case II, unbalanced operation in bus 2. Time scale 3.4 ms/div.



(a) Case I



(b) Case II

Figure 18: Experimental grid signals with method 1. Ch3 grid current i_{ga} (20 A/div). Ch4 grid voltage v_{ga} (200 V/div). ChM FFT for i_{ga} (100 mA/div, Span 10 kHz, Center 4.8 kHz). (a) Case I, balanced operation. (b) Case II, unbalanced operation in bus 2. Time scale 3.3 ms/div.

ent load conditions, therefore, the amplitude of the high frequency components is kept almost constant, increasing its influence on the demanded current. This along the lack of symmetry in the generated voltage, alters the distribution of the harmonics components, shifting the dominant ones to lower orders. This is confirmed in the input current spectrum shown in Figures 18a and 18b, showing that under balance operation, the dominant harmonics of i_{ga} are located in the sidebands around $2m_f$, but in the presence of unbalances, most of the energy is concentrated around m_f, thus are less mitigated by the action of the input filter.

The grid current THD under unbalances reaches a 14.9%, which corresponds to a total demand distortion (TDD) of 7.35%. This is within the admissible limits of the grid code for the

intended power levels ($20 < I_{\mathrm{sc}}/I_{\mathrm{L}} < 50$) [19]. Furthermore, if the unbalanced operation does not exceed one hour in length, it will be considered as a unusual condition and the system will meet the grid code regardless the $I_{\mathrm{sc}}/I_{\mathrm{L}}$ ratio.

7 Conclusion

A novel architecture for a centralized PEVs charging station is proposed, using a bipolar dc grid, enabled by the use of a three level NPC as the central grid-tied converter. The topology allows to operate in the megawatt range without increasing the dc bus voltages, thus maintaining the step down effort of the dc-dc stages of the battery chargers. The NPC enables operation in MV (lower currents, smaller ac chokes) and higher efficiency without compromising power quality.

The limit operation for the selected architecture is demonstrated, showing the incapability of the converter to be able to consume high quality power under any load scenario. If this is not corrected, then the NPC does not represent a viable alternative as the grid-tied converter for a PHEV charging station.

Despite the limitations of the converter to handle unbalanced loads, the formal definition of such condition is used in the proposed controller to overcome this situation, extending the operation range of the converter for any load scenario through the addition of a voltage balancing circuit. In addition, half-wave symmetry is achieved during the whole operation, thus complying with the limits imposed by the grid code.

In this way of balancing the system, the current that needs to be handled by the balancing circuit is just a fraction of the demanded current, putting less stress on the switches and allowing the use of higher switching frequencies, which could reduce the size of the dc inductor.

The distributed dc bus structure allows to reduce the power conversion stages in the system, reducing the costs and improving the overall efficiency. In addition, it facilitates the integration of PV generation and energy storage system, allowing the opportunity to reduce the power demand of the chargers and provide support to the grid.

Finally this structure can be installed in buildings, parking lots, or as conventional filling stations within the cities, enabling alternatives for refueling the PEVs in shorter times, in order to increase its acceptance.

Appendixes

Apendix A: Input current amplitude variation in unbalanced scenarios

In order to determine the amplitude of the fundamental current in any load scenario a power balance of the system is made

$$\frac{3}{2}\text{Re}\left\{\mathbf{v}_s\mathbf{i}_s^*\right\} = \frac{3}{2}R_i\text{Re}\left\{\mathbf{i}_s\mathbf{i}_s^*\right\} + P_d, \tag{24}$$

assuming unity power factor operation (24) can be rewritten in terms of the amplitudes of the signals as

$$\frac{3}{2}V_sI_s = \frac{3}{2}R_iI_s^2 + \frac{V_d}{2}I_{d1}(1+\epsilon), \tag{25}$$

please note that the load on bus one is the rated value. On the other hand, V_d and I_{d1} can be written in terms of the input side quantities as

$$V_d = \frac{\sqrt{3}V_s}{m_a}\sqrt{(1-r_i)^2+l_i^2} \tag{26}$$

$$I_{d1} = \frac{\sqrt{3}}{2}m_aI_{s_{\text{Nom}}}\cos\delta, \tag{27}$$

where r_i and l_i correspond to the per unit values of the input filter resistance and inductance respectively. From the vector diagram shown in Fig. 19, it can be stated that $\cos\delta$ is given by

$$\cos\delta = \frac{1-r_i}{\sqrt{(1-r_i)^2+l_i^2}}. \tag{28}$$

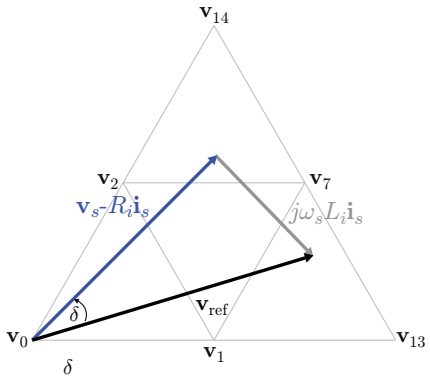


Figure 19: Vector diagram of the system.

Then, replacing (26), (27) and (28) and using the per unit value of the input filter resistance leads to

$$\frac{3}{2}V_s I_s = \frac{3}{2}r_i V_s I_s + \frac{3}{2}V_s I_{s_{\text{Nom}}}(1-r_i)(1+\epsilon). \tag{29}$$

Finally, clearing I_s leads to

$$I_s = \frac{I_{s_{\text{Nom}}}}{2}(1+\epsilon). \tag{30}$$

This result can be generalized, and it models the input current amplitude between the balanced and unbalanced operation for a given fixed load at one of the buses. The approximation is because δ will vary slightly depending on the voltage drop in the input filter and therefore is neglected.

$$I_{s_{\text{un}}} \approx \frac{I_{s_{\text{bal}}}}{2}(1+\epsilon). \tag{31}$$

Remark A1

Please note that the previous analysis was made considering that SVM is being used, explaining the changes in the equations presented in [12], however the same final results are obtained for S-PWM.

Appendix B: Average usage time of the small vectors in 3L-SVM

To have an idea of how much DC drift can be injected under the SVM scheme the following approximation is made. Considering that the balance of the neutral point voltage in this scheme is reduced to the usage of the positive and negative small vectors, and how its dwell-times are distributed, the idea behind this work is to calculate an average value of the remaining time available for this vectors. In other words, in nominal conditions, these vectors are used each sample instant half of the corresponding calculated dwell-time for the small vector t_s, therefore $t_{s_P} = t_{s_N} = 0.5t_s$. Considering this idea, under a certain mid-point voltage drift, the maximum correction that the modulation scheme is able to perform is using either all the dwell-time t_s exclusively for positive (or negative) small vectors. As the dwell times changes depending on the voltage reference angle and its amplitude, an average value will be calculated, in order to have an idea of the maximum DC drift that can be corrected.

To obtain the average time, only the positive half cycle of phase a will be considered, and as the system is symmetrical then extend the results for the remaining phases. Of course this time will depend on the value of the modulation index m_a, as the voltage reference will pass through different regions of the sector depending on its value.

The normalized mean value for the voltage in phase a, during its positive half cycle is defined as:

$$\bar{S}_a \quad = \quad \frac{1}{\pi}\int_0^{\pi} S_a(x)\mathrm{d}x, \tag{32}$$

where S_a corresponds to the switching function of the devices in phase a. This can be used to determine the extra DC drift that can be injected to this voltage by calculating the average time that the small vectors are used $\bar{t}_s$. This time can be redistributed in the limit condition to the exclusive use of certain type of small vectors, therefore there is $\bar{t}_s/2$ left for balancing purposes. This remaining time is equivalent to the maximum DC drift that can be added to the modulating signal.

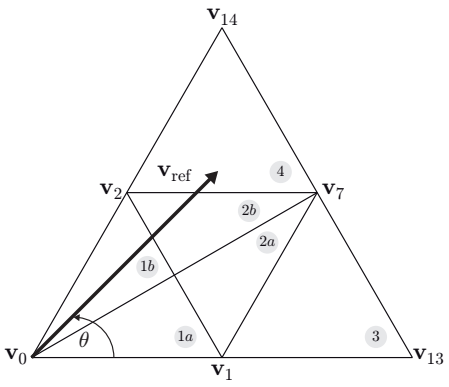


Figure 20: Subdivision in six regions of sector I.

Small modulation index

If $m_a \in [0, 0.5]$, then the reference vector only passes through the regions $1a$ and $1b$ of each sector, as it can be seen from Fig. 20. Then, the associated sectors with the usage of the phase a during the positive half cycle are I, II, V, VI. In order to get the remaining average time, the small vectors that are used in the beginning of the switching sequence are used. This is because, if the vector is located in the beginning (or center) of the switching frequency, it will be alternated with its corresponding negative (or positive) small vector, and this does not occurs if the vector is occupying another position in the switching sequence.

For region I-$1a$ the only small vector that use the phase a is $\mathbf{v}_1$, and its average dwell time is given by

$$\bar{t}_{s_{\mathbf{v}_1}}^{\text{I-}1a} = \int_0^{\theta} 2m_a \sin\left(\frac{\pi}{3} - x\right) \mathrm{d}x \tag{33}$$

then, in region I-$1b$ the vectors are $\mathbf{v}_1$ and $\mathbf{v}_2$ and its corresponding average times, however only $\mathbf{v}_2$ is in the beginning of the sequence ($\mathbf{v}_1$ has already been used the entire time, so there is no time left to use).

$$\bar{t}_{s_{\mathbf{v}_2}}^{\text{I-}1b} = \int_{\frac{\pi}{3}-\theta}^{\frac{\pi}{3}} 2m_a \sin\left(x - \frac{\pi}{3}\right) \mathrm{d}x. \tag{34}$$

For region II-$1a$

$$\bar{t}_{s_{\mathbf{v}_2}}^{\text{II-}1a} = \int_{\frac{\pi}{3}}^{\frac{\pi}{3}+\theta} 2m_a \sin\left(\frac{2\pi}{3} - x\right) \mathrm{d}x. \tag{35}$$

For region V-$1b$

$$\bar{t}_{s_{\mathbf{v}_6}}^{\text{V-}1b} = \int_{\frac{5\pi}{3}-\theta}^{\frac{5\pi}{3}} 2m_a \sin\left(x - \frac{4\pi}{3}\right) \mathrm{d}x. \tag{36}$$

For region VI-$1a$

$$\bar{t}_{s_{\mathbf{v}_6}}^{\text{VI-}1a} = \int_{\frac{5\pi}{3}}^{\frac{5\pi}{3}+\theta} 2m_a \sin\left(2\pi - x\right) \mathrm{d}x. \tag{37}$$

Finally for region VI-$1b$

$$\bar{t}_{s_{\mathbf{v}_1}}^{\text{VI-}1b} = \int_{2\pi-\theta}^{2\pi} 2m_a \sin\left(x - \frac{5\pi}{3}\right) \mathrm{d}x \tag{38}$$

Then, according to (32) and assuming that in this range for m_a $\theta = \pi/6$ the remaining time is given by

$$\frac{\bar{t}_s}{2} = \frac{1}{2\pi}\left(\bar{t}_{s_{\mathbf{v}_1}}^{\text{I-1}a} + \bar{t}_{s_{\mathbf{v}_2}}^{\text{I-1}b} + \bar{t}_{s_{\mathbf{v}_2}}^{\text{II-1}a} + \bar{t}_{s_{\mathbf{v}_6}}^{\text{V-1}b} + \bar{t}_{s_{\mathbf{v}_6}}^{\text{VI-1}a} + \bar{t}_{s_{\mathbf{v}_1}}^{\text{VI-1}b}\right), \tag{39}$$

and, as stated earlier, this is equal to the maximum value for additional DC drift $\hat{\alpha}$, leading to

and this time is equal to the normalized DC drift that can be added to the modulating signal in order to achieve balance, therefore

$$\bar{\alpha} = \frac{-3m_a + 3\sqrt{3}m_a}{\pi}, \tag{40}$$

Medium modulation index

If $m_a \in [0.5, 1/\sqrt{3}]$, then the reference vector passes through the regions $1a$, $1b$, $2a$ and $2b$. In this case θ is the angle at which the reference change the triangle defined by the closest surrounding vectors, and its defined as

$$\theta = \arcsin\left(\frac{1}{2m_a}\right) - \frac{\pi}{3} \tag{41}$$

The expressions for the dwell times in the regions $1a$ and $1b$ have not changed, (33) - (38) are still valid in this range, using the corresponding θ. The remaining dwell times are the following

For region I-$2a$

$$\bar{t}_{s_{\mathbf{v}_1}}^{\text{I-2}a} = \int_{\theta}^{\frac{\pi}{6}} 1 - 2m_a \sin(x)\mathrm{d}x. \tag{42}$$

For region I-$2b$

$$\bar{t}_{s_{\mathbf{v}_2}}^{\text{I-2}b} = \int_{\frac{\pi}{6}}^{\frac{\pi}{3}-\theta} 1 - 2m_a \sin\left(\frac{\pi}{3} - x\right)\mathrm{d}x. \tag{43}$$

For region II-$2a$

$$\bar{t}_{s_{\mathbf{v}_2}}^{\text{II-2}a} = \int_{\frac{\pi}{3}+\theta}^{\frac{\pi}{2}} 1 - 2m_a \sin\left(x - \frac{\pi}{3}\right)\mathrm{d}x. \tag{44}$$

For region V-$2b$

$$\bar{t}_{s_{\mathbf{v}_6}}^{\text{V-2}b} = \int_{\frac{3\pi}{2}}^{\frac{5\pi}{3}-\theta} 1 - 2m_a \sin\left(\frac{5\pi}{3} - x\right)\mathrm{d}x. \tag{45}$$

In region VI-$2a$

$$\bar{t}_{s_{\mathbf{v}_6}}^{\text{VI-2}a} = \int_{\frac{5\pi}{3}+\theta}^{\frac{11\pi}{6}} 1 - 2m_a \sin\left(x - \frac{5\pi}{3}\right)\mathrm{d}x. \tag{46}$$

For region VI-2b

$$\bar{t}^{\text{VI-2}b}_{s_{\mathbf{v}_6}} = \int_{\frac{11\pi}{6}}^{2\pi-\theta} 1 - 2m_a \sin\left(2\pi - x\right) \mathrm{d}x. \tag{47}$$

By adding (33)-(47) and dividing by 2π leads to the average remaining time

$$\hat{\alpha} = \frac{\frac{\pi}{2} - 3m_a - 3\theta - 6m_a\cos(\theta) + 6m_a \sin\left(\theta + \frac{\pi}{6}\right) + 3m_a\sqrt{3}}{\pi} \tag{48}$$

Large modulation index

The remaining modulation index range is $m_a \in [1/\sqrt{3}, 1]$, and the idea behind is the same. In this case, the regions which crosses the reference vector are $2a$, $2b$, 3 and 4. The results in (42) - (47) are still valid in this range, therefore the remaining average times are

In the region I-3

$$\bar{t}^{\text{I-3}}_{s_{\mathbf{v}_1}} = \int_0^{\theta} 2 - 2m_a \sin\left(x + \frac{\pi}{3}\right) \mathrm{d}x. \tag{49}$$

following with region I-4

$$\bar{t}^{\text{I-4}}_{s_{\mathbf{v}_2}} = \int_{\frac{\pi}{3}-\theta}^{\frac{\pi}{3}} 2 - 2m_a \sin\left(x + \frac{\pi}{3}\right) \mathrm{d}x. \tag{50}$$

then, region II-3

$$\bar{t}^{\text{II-3}}_{s_{\mathbf{v}_2}} = \int_{\frac{\pi}{3}}^{\frac{\pi}{3}+\theta} 2 - 2m_a \sin(x) \mathrm{d}x. \tag{51}$$

Finally, region VI-4

$$\bar{t}^{\text{VI-4}}_{s_{\mathbf{v}_1}} = \int_{2\pi-\theta}^{2} \pi 2 - 2m_a \sin\left(x + \frac{4\pi}{3}\right) \mathrm{d}x. \tag{52}$$

Is important to note that in this range, the expression for θ has changed into

$$\theta = \frac{\pi}{3} - \arcsin\left(\frac{1}{2m_a}\right) \tag{53}$$

The average remaining time is then the addition of (42)-(52) divided by 2π, therefore the DC drift injected is defined by:

$$\hat{\alpha} = \frac{\frac{\pi}{2} - 3m_a + 3\theta - 6m_a\cos(\theta) + 6m_a \cos\left(\theta + \frac{\pi}{3}\right) + 3m_a\sqrt{3}}{\pi}. \tag{54}$$

References

[1] M. Yilmaz and P. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *Power Electronics, IEEE Transactions on*, vol. 28, no. 5, pp. 2151–2169, 2013.

[2] L. Dickerman and J. Harrison, "A new car, a new grid," *Power and Energy Magazine, IEEE*, vol. 8, no. 2, pp. 55–61, 2010.

[3] A. Sannino, G. Postiglione, and M. Bollen, "Feasibility of a dc network for commercial facilities," *Industry Applications, IEEE Transactions on*, vol. 39, no. 5, pp. 1499–1507, 2003.

[4] Y. Ito, Y. Zhongqing, and H. Akagi, "Dc microgrid based distribution power generation system," in *Power Electronics and Motion Control Conference, 2004. IPEMC 2004. The 4th International*, vol. 3, 2004, pp. 1740–1745 Vol.3.

[5] S. Bai and S. Lukic, "Design considerations for dc charging station for plug-in vehicles," in *Vehicle Power and Propulsion Conference (VPPC), 2011 IEEE*, 2011, pp. 1–6.

[6] Y. Du, X. Zhou, S. Bai, S. Lukic, and A. Huang, "Review of non-isolated bi-directional dc-dc converters for plug-in hybrid electric vehicle charge station application at municipal parking decks," in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, Feb., pp. 1145–1151.

[7] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped pwm inverter," *Industry Applications, IEEE Transactions on*, vol. IA-17, no. 5, pp. 518 –523, sept. 1981.

[8] N. Celanovic and D. Borojevic, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source pwm inverters," in *Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual*, vol. 1, mar 1999, pp. 535 –541 vol.1.

[9] S. Kouro, J. Rodriguez, B. Wu, S. Bernet, and M. Perez, "Powering the Future of Industry: High-Power Adjustable Speed Drive Topologies," *Industry Applications Magazine, IEEE*, vol. 18, no. 4, pp. 26–39, 2012.

[10] T. Kaipia, P. Salonen, J. Lassila, and J. Partanen, "Possibilities of the low voltage DC distribution systems," in *Nordic Distribution Automation Conference (NORDAC)*, 2006.

[11] H. Kakigano, Y. Miura, T. Ise, and R. Uchida, "Dc voltage control of the dc micro-grid for super high quality distribution," in *Power Conversion Conference - Nagoya, 2007. PCC '07*, 2007, pp. 518–525.

[12] A. Yazdani and R. Iravani, "A generalized state-space averaged model of the three-level NPC converter for systematic DC-voltage-balancer and current-controller design," *Power Delivery, IEEE Transactions on*, vol. 20, no. 2, pp. 1105–1114, 2005.

[13] Z. Mohzani, B. McGrath, and D. Holmes, "The balancing properties of dc link compensation for 3-phase neutral point clamped (npc) converter," in *Power Electronics and Motion Control Conference (IPEMC), 2012 7th International*, vol. 1, 2012, pp. 574–579.

[14] J. Moia, J. Lago, A. Perin, and M. Heldwein, "Comparison of three-phase pwm rectifiers to interface AC grids and bipolar DC active distribution networks," in *Power Electronics for Distributed Generation Systems (PEDG), 2012 3rd IEEE International Symposium on*, 2012, pp. 221–228.

[15] H. Akagi, H. Fujita, S. Yonetani, and Y. Kondo, "A 6.6-kV transformerless STATCOM based on a five-level diode-clamped PWM converter: system design and experimentation of a 200-V, 10-kVA laboratory model," in *Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005*, vol. 1, 2005, pp. 557–564 Vol. 1.

[16] B. Wu, *High-Power converters and AC drives*, M. E. El-Hawary, Ed. Wiley - IEEE Press, April 2006.

[17] D. Feng, B. Wu, C. Liu, D. Xu, and R. Cheung, "Space Vector Modulation for High-Power Three-Level NPC Rectifiers Without Even Order Harmonics," in *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th*, 2005, pp. 1986–1991.

[18] S. Rivera, B. Wu, J. Wang, S. Kouro, and H. Athab, "Electric Vehicle Charging Station using a Neutral Point Clamped Converter with Bipolar dc Bus and Voltage Balancing Circuit," in *IECON 2013 - 39th Annual Conference on IEEE Industrial Electronics Society*, november 2013.

[19] "IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems," *IEEE Std 519-1992*, 1993.