Effective Voltage Balance Control for Bipolar-DC-Bus-Fed EV Charging Station With Three-Level DC–DC Fast Charger

Longcheng Tan, Bin Wu, *Fellow, IEEE*, Venkata Yaramasu, *Member, IEEE*, Sebastian Rivera, *Student Member, IEEE*, and Xiaoqiang Guo, *Senior Member, IEEE*

***Abstract*—The development of high-power charging stations with fast chargers is a promising solution to shorten the charging time for electric vehicles (EVs). The neutral-point-clamped (NPC) converter-based bipolar-dc-bus-fed charging station brings many merits, but it has inherent voltage balance limits. To solve this issue, a voltage balance control (VBC) method based on a new modulation together with three-level (TL) dc–dc converter-based fast charger is proposed. Additionally, an effective VBC coordination between the TL dc–dc converter and the NPC converter is formulated. Through the proposed VBC coordination, the controllable balancing region is extended so that additional balancing circuits are eliminated. Meanwhile, the quality of the grid-side currents is improved as the NPC converter has more freedom to control currents. The low-frequency voltage fluctuations in dc buses are removed because the TL dc–dc converter performs most of the balancing tasks. Faster VBC perturbation performance is achieved due to higher available balancing current at TL dc–dc converter side. In addition, the voltage balance limits of both the TL dc–dc converter and the NPC converter are explored. The voltage balancing performances are compared when VBC is located at different sides. Simulation and experimental results are provided to verify the proposed VBC and the VBC coordination.**

***Index Terms*—Electric vehicles (EVs), fast charger, neutral-point-clamped (NPC) converter, three-level (TL) dc–dc converter, voltage balance control (VBC).**

I. Introduction

With more attention paid to the increasing greenhouse emission and the gradual exhaustion of fossil fuel, plug-in hybrid electric vehicles (PHEVs) and electric vehicles (EVs) have emerged as a viable alternative to the conventional internal combustion engine vehicles (ICEVs) [1]–[4]. However, the long charging time and the limited range per charge are still challenging problems impeding the widespread acceptance of PHEVs and EVs. In order to solve these problems, the concept of building high-power charging stations with fast chargers is a promising solution [2], [5]–[7].

There are two basic architectures for the charging station to integrate all fast chargers into a common bus [6], [7]. 1) The common ac-bus architecture, which needs all the fast chargers having dedicated ac–dc conversion stages. 2) The common dc-bus architecture, which only needs a central ac–dc conversion stage. Taking into account the characteristics of EV batteries and possible integration of renewable energy sources into the system, the latter configuration exhibits considerable advantages, because of the dc power requirement of EV battery chargers and the absence of synchronization issues of integrating renewable sources, leading to less-conversion stages and higher system efficiency [6]–[9].

The common dc-bus can be provided by a conventional two-level voltage-source converter, or by a neutral-point-clamped (NPC) converter. The latter bipolar-dc-bus architecture has merits over the former unipolar one, as the NPC converter can withstand higher system voltage, handle more power, have better power quality, and offer more flexible ways for the loads to be connected to the bipolar dc bus [7]. However, as the NPC converter has inherent voltage balance limits and the occurrences of EV charging is random, the bipolar-dc-bus architecture cannot guarantee the dc-bus voltages balanced during all the operating conditions [7], [10]. The unbalanced voltages are undesirable as they affect the power quality, increase the voltage stress of semiconductor devices, and, in the worst case scenario, cause severe damage to overall power conversion units. In order to solve this problem, additional balancing circuits are required at an expense of higher system cost and degraded efficiency [7].

On the other hand, in order to shorten the charging time, it is necessary to develop fast chargers with high-power ratings. The SAE International has drafted the fast charger configurations (Level III) with dc voltage up to 600 V and dc current up to 550 A in order to charge EVs within acceptable time [5], [11]–[14]. In order to meet the high-power requirement, the multiphase interleaved buck converter has been introduced in [15]–[18] for fast chargers to share the high charging power between multiple modules. The isolated soft-switching dc–dc converters have also been discussed in

Manuscript received January 22, 2015; revised October 6, 2015 and December 23, 2015; accepted February 5, 2016. Date of publication March 8, 2016; date of current version June 9, 2016. This work was supported by Toronto Hydro (THESL) through Project TH1302 at the Centre for Urban Energy, Ryerson University.

L. Tan, B. Wu, and S. Rivera are with the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, M5B 2K3, Canada (e-mail: ltan@ee.ryerson.ca; bwu@ee.ryerson.ca; srivera@ee.ryerson.ca).

V. Yaramasu is with the Department of Electrical Engineering and Computer Science, Northern Arizona University, Flagstaff, AZ 86001 USA (e-mail: Venkata.Yaramasu@nau.edu).

X. Guo is with the Department of Electrical Engineering, Yanshan University, Qinghuangdao 66004, China (e-mail: gxq@ysu.edu.cn).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIE.2016.2539248

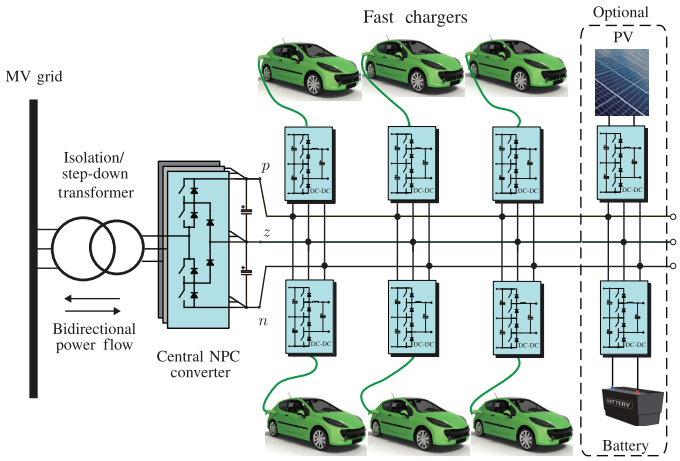

Fig. 1. Configuration of the bipolar-dc-bus-fed EV charging station.

[19]–[21] for the high-power charging applications. Although the aforementioned topologies have respective advantages, when the bipolar-dc-bus-fed charging station with an isolation transformer at the grid side is chosen (as shown in Fig. 1), the three-level (TL) nonisolated dc–dc converter is more suitable, as it can be directly connected to the bipolar dc bus, and there is no need for a high-frequency isolation transformer.

The TL nonisolated dc–dc converter has been widely applied in high-voltage high-power applications so as to reduce the device voltage stress, to increase the power ratings, and to decrease the output filter size compared to the two-level dc–dc converters [22]–[28]. Similar to the NPC converter, the premise of proper operation for TL dc–dc converter also needs the balance of dc-side capacitor voltages. Different voltage balance control (VBC) methods have been studied in literature: 1) a VBC method based on the state machine modulation is analyzed in [22]; 2) a classic VBC method using a phase-shifted pulsewidth modulation (PWM) is introduced in [23] and [24]; and 3) a predictive balance controller through the minimization of cost function is discussed in [25]. However, few of them studied the case when TL dc–dc converters are connected to a central NPC converter as shown in Fig. 1. The VBC coordination between them is still not addressed in literatures and the voltage balance limits of TL dc–dc converters are not yet explored.

This paper first proposes an effective VBC along with a new modulation for the high-power TL dc–dc converter-based fast charger. The proposed VBC always utilizes the maximum available output current to perform balancing tasks so that faster balancing response is obtained. Second, the voltage balance limits of both the TL dc–dc converter and the NPC converter are explored and the VBC coordination between them is investigated so as to extend the controllable balancing region and remove any additional balancing circuits. The voltage balancing performances are compared when VBC is located at the TL dc–dc converter side and the NPC converter side. Simulation and experimental results are presented to verify the proposed VBC and the VBC coordination in EV charging station.

II. Proposed Modulation for TL DC–DC Converter

The topology of TL dc–dc converter is presented in Fig. 2(b), which is composed of four switches S_1, S_2, S_3, S_4; along with four freewheeling diodes D_1, D_2, D_3, D_4; input filter capacitors C_i; the output filter inductor L_o; and capacitor C_o. The three connection points p, z, n at the input side allow to directly connect TL dc–dc converter to the central NPC converter [refer to Fig. 2(a)].

The proposed modulation scheme and operating principle are shown in Figs. 3 and 4, corresponding to the modulation signal (duty cycle generated by the controller) $d \leq 0.5$ and $d > 0.5$, respectively. The modulation signals d_1 and d_4 are compared with the carrier signal c to generate gate signals for outer two switches S_1 and S_4, while the inner switches S_2 and S_3 operate in a complementary manner to their neighboring outer switches. The modulation signals d_1 and d_4 are obtained according to the amplitude of modulation signal d and the selected switching sequence types (P- or N-type). These sequences are defined on the basis of the positive or negative polarity of the generated average neutral-point current i_{np}.

The relationship between d_1, d_4, and d is expressed in the following equations:

$$\begin{cases} d_1 = 2d, d_4 = 0, & \text{for } 0 \leq d \leq 0.5 \text{ and N-type} \\ d_4 = 2d, d_1 = 0, & \text{for } 0 \leq d \leq 0.5 \text{ and P-type} \end{cases} \quad (1)$$

$$\begin{cases} d_1 = 1, d_4 = 2d - 1, & \text{for } 0.5 \leq d \leq 1 \text{ and N-type} \\ d_4 = 1, d_1 = 2d - 1, & \text{for } 0.5 \leq d \leq 1 \text{ and P-type.} \end{cases} \quad (2)$$

The comparison between modulation signals and the carrier signal leads to four switching states: 14, 13, 23, and 24, where the numbers denote the conducting switches. For example, 14 means S_1, S_4 are turned "on." To simplify the analysis of the operation principle, it is assumed that the capacitor voltages are equal, i.e., $v_{i1} = v_{i2} = v_i$. With this assumption, the state 14 has the output voltage of total dc voltage $2v_i$; state 23 has zero output voltage; while states 13 and 24 have half the total dc-bus voltage v_i. This phenomena leads to three voltage levels (0, v_i, and $2v_i$) in the output voltage waveform v_g. Fig. 5 illustrates the switching sequences when the duty cycle changes from $d \leq 0.5$ with N-type to $d > 0.5$ with P-type, it can be seen that there are three voltage levels appearing at the output voltage v_g, and the average neutral-point current i_{np} changes from negative to positive.

Two different switching sequences are proposed for $d \leq 0.5$ as shown in Fig. 3, one of which is N-type with states changing among 23 and 13, while the other one is P-type with states transiting between 23 and 24. Similarly, N- and P-type sequences are also proposed for $d > 0.5$ with their states switching between 13 and 14 or 24 and 14. Since the N-type sequence has negative average neutral-point current, and the P-type sequence has positive average neutral-point current, they have opposite balancing effects on the capacitor voltages, thereby it can be used toward the voltage balance tasks.

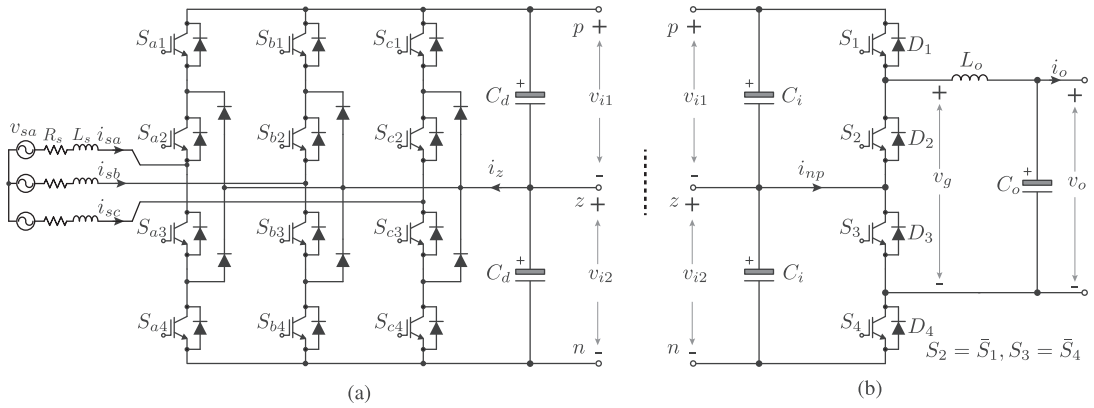

Fig. 2. Block diagram of (a) central NPC converter and (c) TL dc–dc converter.

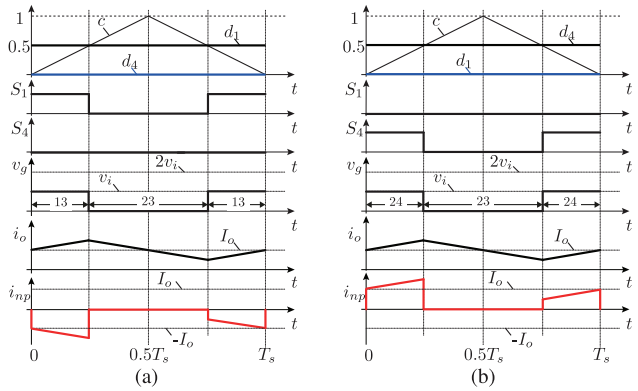

Fig. 3. Modulation principle of TL dc–dc converter for $d \leq 0.5$. (a) N-type. (b) P-type.

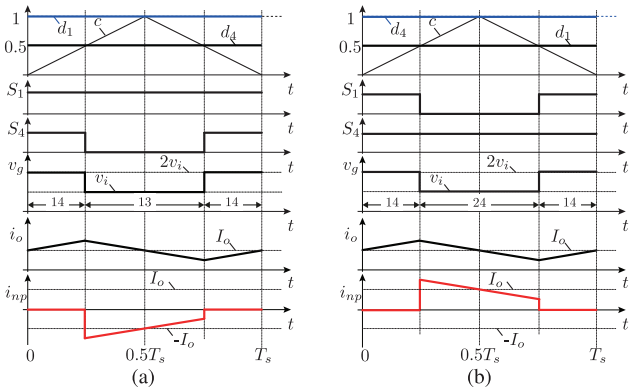

Fig. 4. Modulation principle of TL dc–dc converter for $d > 0.5$. (a) N-type. (b) P-type.

Based on Figs. 3 and 4, the output current i_o for $d \leq 0.5$ is given by

$$i_o(t) = \begin{cases} I_o + \dfrac{\Delta i_o}{2dT_s}t, & kT_s \leq t \leq (k+d)T_s \\ I_o - \dfrac{\Delta i_o(2t - T_s)}{2(1-2d)T_s}, & (k+d)T_s \leq t \leq (k+1-d)T_s \\ I_o + \dfrac{\Delta i_o}{2dT_s}(t - T_s), & (k+1-d)T_s \leq t \leq (k+1)T_s \end{cases} \tag{3}$$

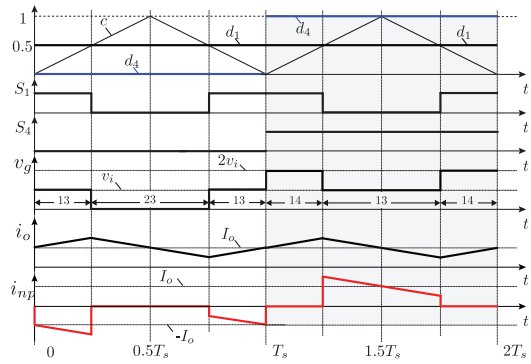

Fig. 5. Switching sequences from N-type $d < 0.5$ to P-type $d > 0.5$.

where T_s is the carrier period, k is a positive integer ($k \in [0, +\infty)$), I_o is the average output current, and Δi_o is the output current ripple, which can be modeled as

$$\Delta i_o = \begin{cases} 2d(1-2d)T_s v_i / L_o, & d \leq 0.5 \\ 2(1-d)(2d-1)T_s v_i / L_o, & d > 0.5. \end{cases} \tag{4}$$

Assume that the duty cycle is d, and the output current polarity is positive. From Figs. 3 and 4, the average output voltage is obtained

$$v_o = \int_0^{T_s} v_o(t)dt = 2v_i d, \quad v_o(t + T_s) = v_o(t). \tag{5}$$

As shown in (5), the output voltage is proportional to the duty cycle d and it is a periodic function with period T_s, which indicates that the effective fundamental frequency of the output voltage v_o equals the switching frequency f_s.

In order to compare with the modulation introduced in [23], Fig. 6 gives the modulation principles for both methods, and the output current ripple for modulation in [23] can be obtained similarly

$$\Delta i_o = \begin{cases} d(1-2d)T_d v_i / L_o, & d \leq 0.5 \\ (1-d)(2d-1)T_d v_i / L_o, & d > 0.5 \end{cases} \tag{6}$$

where T_d is the carrier period for modulation in [23].

Compare (4) and (6), it can be found that in order to obtain the same current ripple, the carrier period T_s of the proposed modulation should be half of the carrier period T_d in modulation [23]. However, as shown in Fig. 6(a), because only one

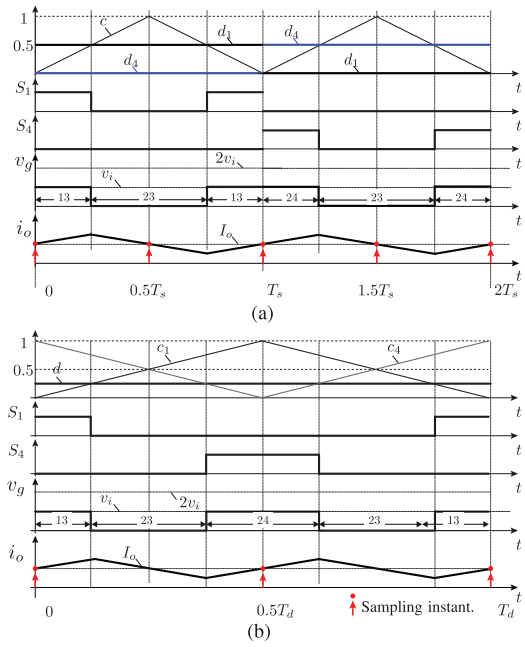

Fig. 6. Comparison between switching sequences and sampling instants for (a) proposed modulation and the (b) one in [23].

pair of switches change their states while the other pair keep unchanged in the proposed modulation, the actual switching frequencies of the two modulations are the same.

Fig. 6 also demonstrates the sampling instants for both modulations considering that the asymmetric uniform sampling technique is used. It can be seen that the effective sampling frequency of the proposed method is two times as the conventional one when $T_s = 0.5T_d$. Based on the zero-order hold effect of modulations, the PWM delay can be modeled in (7), where T_x is the sampling period. It indicates that the proposed modulation has reduced PWM delay, as the effective sampling frequency is two times as the one in [23], i.e., $T_s = 0.5T_d$, leading to improved control dynamics and increased control bandwidth [29]–[31]

$$G_h(s) = \frac{1 - e^{-s \cdot T_x}}{s} \approx T_x e^{-s \cdot 0.5 T_x}. \tag{7}$$

III. VBC for TL DC–DC Converter and NPC Converter

A. Proposed VBC

To illustrate the voltage balancing principle, assume that the output current of the TL dc–dc converter is positive, and the total dc-side voltage is fixed to $2v_i$. The output filter capacitor along with the battery load is represented by an ideal voltage source. The resulting equivalent circuits are shown in Fig. 7 for the four possible switching stages. As mentioned in previous sections, the switching stages 23 and 14 have no impact on VBC as there is no current flowing through the neutral-point z, while switching stages 13 and 24 have opposite impacts on the VBC: stage 13 discharges the upper capacitor while stage 24 discharges the lower capacitor.

Based on this feature and the proposed modulation, the VBC principle is formulated: if the upper capacitor voltage v_{i1} is greater than the lower capacitor voltage v_{i2}, then the N-type switching sequence is chosen to discharge the upper capacitor. Similarly, if v_{i1} is smaller than v_{i2}, then the opposite choice is selected, i.e., the P-type switching sequence, is chosen to discharge the lower capacitor. When the capacitor voltages are balanced, the P- and N-type switching sequences are chosen alternatively in order to achieve zero average neutral-point current. Because the proposed VBC always uses the maximum available output current to perform the balancing task, its balancing performance is enhanced. The same analysis is repeated for the case when the output current is negative.

B. Voltage Balance Limits of TL DC–DC Converter

In order to fully utilize the VBC ability of the TL dc–dc converter, the voltage balance limits have to be explored. Based on Figs. 3 and 4, the maximum average neutral-point current i_m provided by the converter is formulated

$$i_m = \begin{cases} 2di_o, & d \le 0.5 \\ 2(1-d)i_o, & d > 0.5 \end{cases} \tag{8}$$

then the maximum unbalanced power p_m between the upper and the lower dc buses that can be handled by the TL dc–dc converter is defined by

$$p_m = \begin{cases} p_o, & d \le 0.5 \\ (1/d - 1)p_o, & d > 0.5. \end{cases} \tag{9}$$

Therefore, the unbalanced power ratio η_d between the maximum unbalanced power p_m and the output power p_o is expressed as

$$\eta_d = \begin{cases} 1, & d \le 0.5 \\ 1/d - 1, & d > 0.5. \end{cases} \tag{10}$$

Finally, based on (10), the voltage balance limits of TL dc–dc converter are plotted in Fig. 8(a), where the shaded area is the controllable balancing region which can be achieved by the TL dc–dc converter.

C. Voltage Balance Limits of NPC Converter

The classic VBC principle for NPC converter is adopted from the works in [7] and [32], where a linear PI controller is used to regulate the dwell time allocation for redundant small vectors as shown in the following equation:

$$t_{ap} = \frac{t_a}{2}(1 - \Delta t), \quad t_{an} = \frac{t_a}{2}(1 + \Delta t) \tag{11}$$

where Δt is the actuation of the PI controller.

In [7], the maximum unbalanced condition for which the modulation is able to keep the voltages from drifting is defined. This is done in terms of the minimal power ratio $\hat{\varepsilon}$ between the upper and the lower dc buses. This ratio is defined as

$$\hat{\varepsilon} = \frac{2\sqrt{3}m}{\sqrt{3}m + \frac{6\hat{\alpha}}{\pi}} - 1 \tag{12}$$

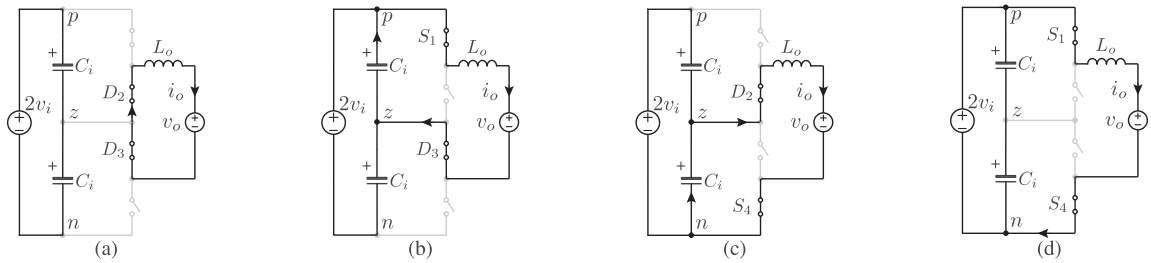

Fig. 7. Four operating stages of TL dc–dc converter and their equivalent circuits. (a) 23. (b) 13. (c) 24. (d) 14.

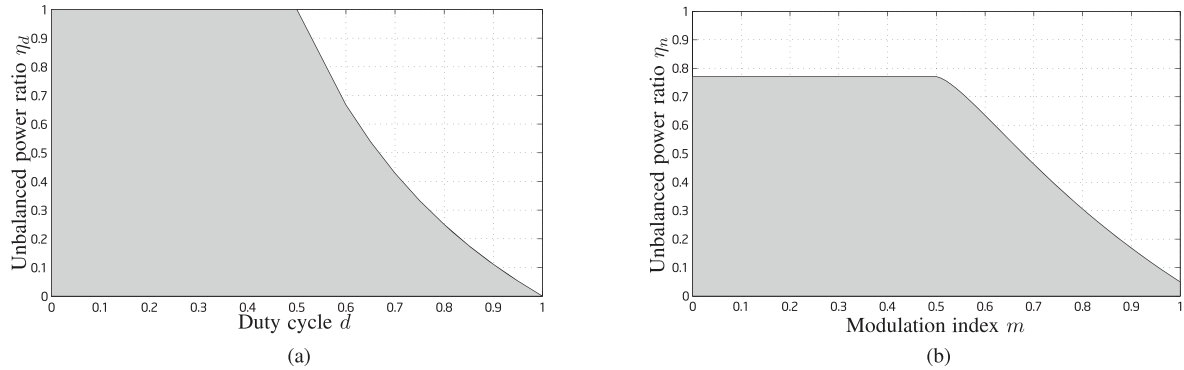

Fig. 8. Voltage balance limits of (a) TL dc–dc converter and (b) NPC converter.

where m is the modulation index of NPC converter and $\hat{\alpha}$ is the maximum voltage drift that can be injected by redistributing the dwell time allocation for redundant small vectors.

However, in order to compare with the voltage balance limits of TL dc–dc converter, this condition is expressed in terms of unbalanced power ratio η_n between the maximum unbalanced power and the output power leading to

$$\eta_n = \frac{1-\hat{\varepsilon}}{1+\hat{\varepsilon}} \tag{13}$$

then, based on (12) and (13) and [7], the voltage balance limits of NPC converter is presented in Fig. 8(b), where the shaded area is the controllable balancing region of the NPC converter.

IV. Coordinated VBC

A. Coordination Principle

By comparing Fig. 8(a) and (b), it is found that the controllable balancing regions of both the TL dc–dc converter and NPC converter cannot cover the whole operating range. Especially, for the TL dc–dc converter, the maximum balance power P_b is equal to the output power P_o when duty cycle $d \leq 0.5$, but inversely proportional to duty cycle d when $d > 0.5$. On the other hand, for the NPC converter, the maximum balance power P_b is $0.7708\,P_o$ when modulation index $m \leq 0.5$, but decreases gradually as the modulation index increases from 0.5 to 1. In practice, the NPC converter usually operates around $m = 0.9$ to maximize the dc voltage utilization; therefore, the balance power provided by the NPC converter is around $0.2\,P_o$. Meanwhile, it should be noticed that the TL dc–dc converter cannot provide any balance power when it is not working. Therefore, in order to extend the controllable balancing region and eliminate any additional balancing circuit, the coordinated VBC between the NPC converter and the TL dc–dc converter is established in this paper.

Based on the proposed VBC for TL dc–dc converter and the classic VBC for NPC converter, the proposed coordination rule between them is formulated as follows: 1) when there are no fast chargers working, i.e., $P_o = 0$, the NPC converter performs the VBC task; 2) when the fast chargers are in operation and the unbalanced power ratio η is within their controllable balance region, i.e., $\eta < \eta_{dm}$, then TL dc–dc converters perform the VBC task alone; and 3) when the fast chargers are in operation and the unbalanced power ratio η is over their controllable balance region but within the overall controllable balance region of charging station, i.e., $\eta < \eta_{dm} + \eta_{nm}$, both the TL dc–dc converters and NPC converter are responsible for the VBC tasks. The explicit cooperation rules are defined as follows:

$$\begin{cases} i^*_{np} = 0, & \Delta t = \Delta t_0, \text{when } P_o = 0 \\ i^*_{np} = i^*_{np0}, \Delta t = 0, & \text{when } \eta < \eta_{dm} \\ i^*_{np} = i^*_{np0}, \Delta t = \Delta t_0, & \text{when } \eta_{dm} < \eta < \eta_{dm} + \eta_{nm} \end{cases} \tag{14}$$

where η is the unbalanced power ratio of loads, η_{dm} and η_{nm} are the maximum controllable balancing limits of the TL dc–dc converter and NPC converter, respectively. i^*_{np0} and i^*_{np} are the original and modified neutral-point current reference for the TL dc–dc converter. Δt_0 and Δt are the original and modified adjusting time interval for redundant small vectors of the NPC converter. $\Delta t = 0$ means VBC is deactivated at the NPC converter side. $i^*_{\text{np}} = 0$ indicates VBC is deactivated at the TL dc–dc converter side.

After collecting voltages and currents information of all fast chargers connected to the bipolar dc bus of a charging station,

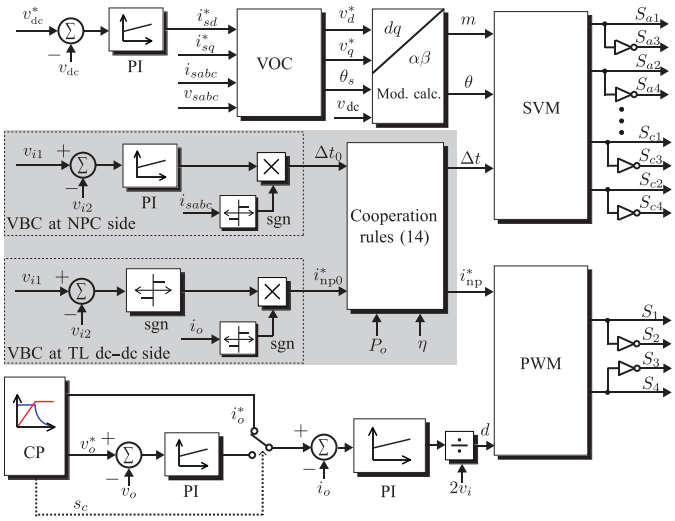

Fig. 9. System control diagram with coordinated VBC.

TABLE I
PARAMETERS FOR NPC CONVERTER

Paramenter	Sym.	Sim. value	Exp. value
Input inductance (p.u.)	L_s	0.25	0.24
Input resistance (p.u.)	R_s	0.01	0.01
DC-link capacitance (p.u.)	C_d	3.04	3.05
Switching frequency (p.u.)	f_s	18	18
Base frequency (Hz)	$f_{\rm B}$	60	60
Base voltage (V)	$V_{\rm B}$	960	68
Base power (kW)	$P_{\rm B}$	240	1.2

TABLE II
PARAMETERS FOR TL DC–DC CONVERTER

Paramenter	Sym.	Sim. value	Exp. value
Input capacitance (p.u.)	C_i	0.56	0.56
Output inductance (p.u.)	L_o	1.25	1.25
Output capacitance (p.u.)	C_o	0.67	0.67
Switching frequency (p.u.)	f_s	36	36
Base frequency (Hz)	$f_{\rm B}$	60	60
Base voltage (V)	$V_{\rm B}$	600	42
Base power (kW)	$P_{\rm B}$	240	1.2

it is required to calculate the unbalanced power ratio and the necessary balancing power. With this information, it is feasible to allocate the balancing tasks among operating fast chargers and the NPC converter. It should be noted that since the charging station only has fast chargers as its loads, and all the fast chargers have the VBC abilities, they ensure balanced power operation among the bipolar dc bus in addition to the VBC assistance. Therefore, through the coordination, the controllable balancing region is extended to all the operating range so that additional balancing circuits can be eliminated. Meanwhile, the grid-side current quality can also be improved because the NPC converter has more freedom to control grid-side currents [25].

B. Control Scheme

The system control scheme for the TL dc–dc converter along with the central NPC converter is shown in Fig. 9. The constant current (CC) and constant voltage (CV) charging methods are adopted in the system, as shown in the left bottom part of Fig. 9, where the charging profile (CP) provides the reference current i_o^*, the reference voltage v_o^*, and the switch signal s_c to control the transition between CC and CV charging modes on the basis of the real battery charging process. The converter output current is regulated using a PI controller, and its output is divided by the total input dc voltage $2v_i$ to generate the modulation signal d. For the NPC converter, the total dc-side voltage v_{dc} is controlled through a PI controller, and the input currents are controlled through the classic grid-voltage-oriented control (VOC) [33], then the amplitude m and angle θ of the modulation vector for the NPC converter are obtained.

The proposed VBC for the TL dc–dc converter is shown in lower dashed-line box in the shaded area of Fig. 9, where the difference between upper capacitor voltage v_{i1} and lower capacitor voltage v_{i2} is passed through a comparator or a *sign* detector, then the output of it is multiplied by the sign of output current to get the required original neutral-point current $i_{\rm np0}^*$. Similarly, the classic VBC for NPC converter is demonstrated in upper dashed-line box in the shaded area, where the voltage difference is controlled through a PI controller, and the output of it is multiplied by the sign of grid-side currents selectively to get the required original adjusting time interval Δt_0 [32].

Then, the final neutral-point reference current $i_{\rm np}^*$ and regulated dwell time Δt are obtained by passing their original values $i_{\rm np0}^*$ and Δt_0 through the cooperation rules expressed in (14). Δt is used to adjust the dwell time of redundant small vectors for the NPC converter [32], thus is given to the SVM algorithm to generate the gating signals S_{a1} to S_{c4}. On the other hand, for the TL dc–dc converter, if $i_{\rm np}^* < 0$, the N-type sequence is selected; if $i_{\rm np}^* > 0$, the P-type sequence is selected; and if $i_{\rm np}^* = 0$, the P- and N-type sequences are selected alternatively. Then, based on the modulation signal d, the selected P- or N-type switching sequence, and through the proposed modulation technique discussed earlier in Section II, the gating signals S_1, S_2, S_3, and S_4 are obtained.

V. SIMULATION RESULTS

The proposed VBC for the TL dc–dc converter-based fast charger and the coordinated VBC for the charging station system is simulated using MATLAB/Simulink software. A 240-kW system is designed for validation, where the detailed system parameters of the NPC converter and the TL dc–dc converter are shown in Tables I and II, respectively.

The total dc-bus voltage (between p and n) is controlled to be 1600 V through the central NPC converter. In order to verify the proposed VBC and its coordination, two different resistors (9.4 and 12.2 Ω) are connected across upper and lower capacitors to create the unbalanced power between the bipolar dc buses on purpose.

A. Steady-State Analysis

The steady-state performance is analyzed and compared when VBC is located at different sides, as presented in Fig. 10. Fig. 10(a)(i) demonstrates that there are low-frequency voltage

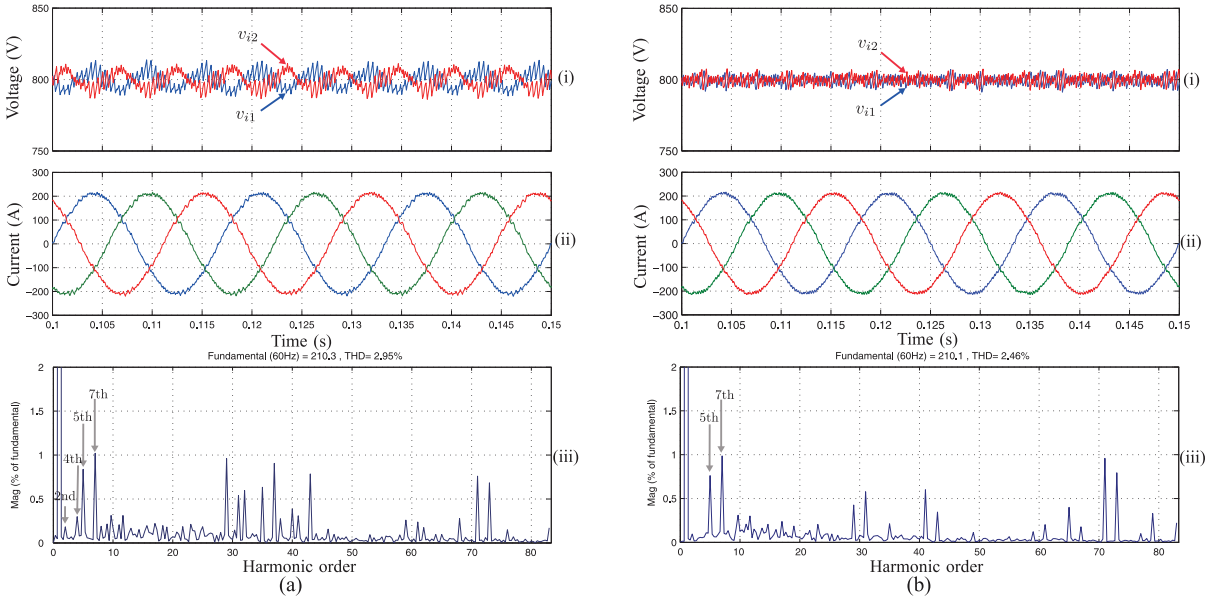

Fig. 10. Simulated steady-state performance comparison for VBC at different sides. (i) Upper capacitor voltage v_{i1} and lower capacitor voltage v_{i2}. (ii) Grid-side currents i_{sa}, i_{sb}, i_{sc}. (iii) FFT analyses of grid-side currents. (a) VBC at NPC converter side. (b) VBC at TL dc–dc converter side.

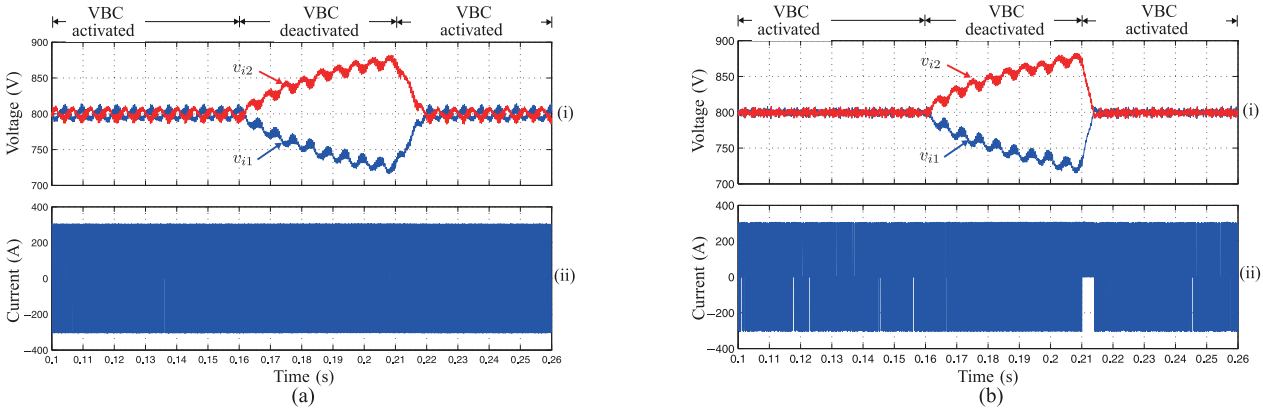

Fig. 11. Simulated perturbation performance comparison for VBC at different sides. (i) Upper capacitor voltage v_{i1} and lower capacitor voltage v_{i2}. (ii) Neutral-point current of the TL dc–dc converter. (a) VBC at NPC converter side. (b) VBC at TL dc–dc converter side.

fluctuations at the dc side when only the NPC converter takes charge of the VBC task, which is an inherent characteristic of NPC converter due to the waveform of the neutral-point current [10], [34]. On the contrary, as shown in Fig. 10(b)(i), the dc voltages are perfectly balanced without any low-frequency voltage fluctuations when VBC is located at TL dc–dc converter side.

In addition, by comparing Fig. 10(a)(ii) and (b)(ii), it can be found that the grid-side current quality is improved when VBC is located at TL dc–dc converter side, which can be verified further by comparing the FFT analyses shown in Fig. 10(a)(iii) and (b)(iii). The FFT analyses indicate that when VBC is located at the NPC converter side, the THD of grid-side currents is 2.95%, higher than 2.46% when VBC at TL dc–dc converter side, and the even-order harmonics such as the second and fourth harmonics also appear. The presence of even-order harmonics is not desirable at the grid side since they are strictly regulated by the IEEE Standards 519-1992 [32]. Therefore, the proposed VBC coordination not only eliminates the low-frequency voltage fluctuations of the dc bus, but also improves the grid-side power quality.

B. Disturbance Response

This section verifies the disturbance response of the proposed VBC for TL dc–dc converter, and compares the disturbance rejection performance when VBC is performed at different sides. The VBC is performed first at the NPC converter side from 0.1 to 0.26 s but during which the VBC is deactivated from 0.16 to 0.21 s on purpose. On the contrary, the VBC is then performed at the TL dc–dc converter side and the same disturbance process is simulated. Fig. 11(b) demonstrates the performance of the proposed VBC for TL dc–dc converter, and it can be seen that the upper capacitor voltage v_{i1} and lower capacitor voltage v_{i2} diverge during the VBC deactivation period, but they converge quickly after the reactivation of VBC and keep

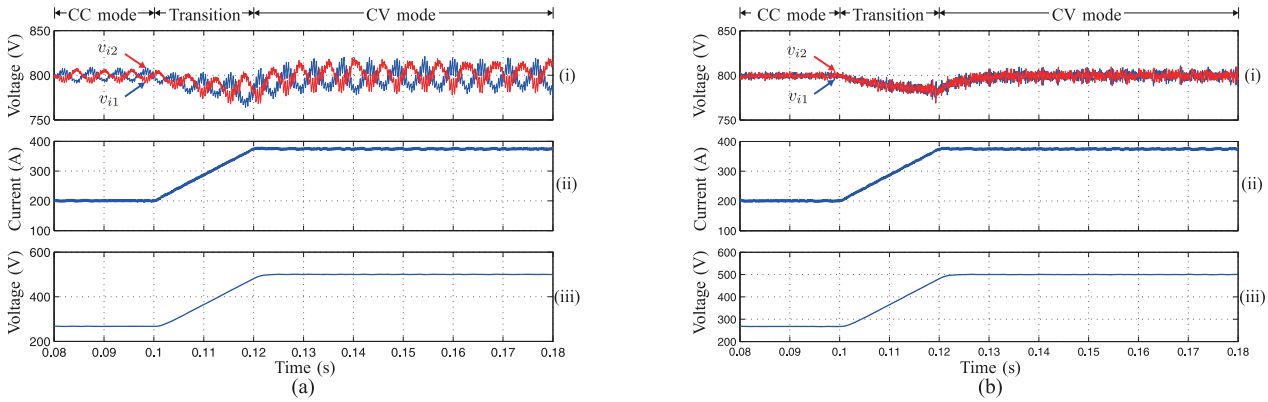

Fig. 12. Simulated transient performance for VBC at different sides from CC mode to CV mode. (i) Upper capacitor voltage v_{i1} and lower capacitor voltage v_{i2}. (ii) Output current i_o. (iii) Output voltage v_o. (a) VBC at NPC converter side. (b) VBC at TL dc–dc converter side.

balanced with less steady-state error during all the following VBC-activated period.

By comparing Fig. 11(a) with (b), it can be seen that although the NPC converter can make the two capacitor voltages converge after reactivating the VBC, the response speed of the proposed VBC at the TL dc–dc converter side is faster, because the proposed VBC at TL dc–dc converter side uses the whole output current (300 A) to balance the dc-bus voltages as shown in Fig. 11(b)(ii). On the contrary, due to its inherent balance limits, the NPC converter can only utilize part of the fundamental grid-side currents to perform the balancing task [10], [34]. For this simulation case, the available average neutral-point current of the NPC converter for balancing task is around 71 A, which is 35% of grid-side current of 204 A. Therefore, theoretically, the proposed VBC at the TL dc–dc converter side is faster than the VBC at NPC converter side, because the available average balancing current is higher.

C. Transient Response

In order to compare the transient response when VBC is located at different sides, the whole transition process from the CC charging mode ($i_o^* = 200\,A$) to the CV charging mode ($v_o^* = 500\,V$) is simulated. Fig. 12(a) illustrates the simulated transient performance when VBC is located at NPC converter side, while Fig. 12(b) shows the simulated transient results when VBC is at TL dc–dc converter side. It can be seen that under both conditions, the output current i_o and the output voltage v_o track their references with zero steady-state error, and the transition process is also very smooth without any overshoots.

However, by comparing Fig. 12(a)(i) with (b)(i), it can be seen that the capacitor voltages have reduced ripples and no significant low-frequency fluctuations when VBC is located at TL dc–dc converter side, which is beneficial to the capacitors lifetime.

The above simulation results verify the proposed VBC for TL dc–dc converter, and also validate the benefits of the coordinated VBC between the TL dc–dc converter and the NPC converter, which brings improved grid-side currents quality, faster voltage balancing response, and enhanced voltage balancing performance.

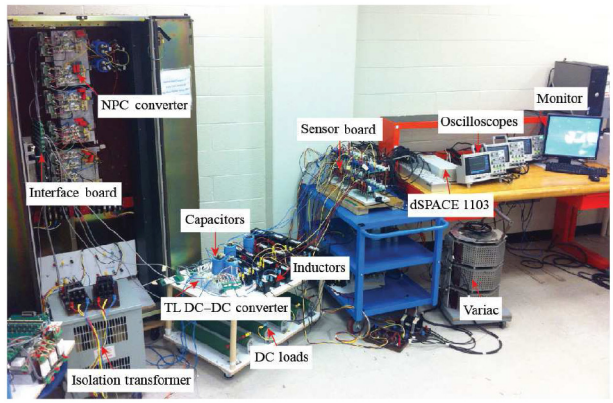

Fig. 13. Photograph of the experimental setup.

VI. Experimental Results

In this section, the proposed VBC for the TL dc–dc converter and the coordinated VBC scheme are verified through experimental tests. In order to perform the experiment, a 1.2-kW setup composed of a central NPC converter and a TL dc–dc converter has been built (refer to Fig. 13 for the photograph of setup). The parameters of the NPC converter and TL dc–dc converter are given in Tables I and II. The control platform is based on a dSPACE 1103 which samples the voltages and currents through the sensor boards, performs the control algorithms and PWM, then sends the gating signals for the IGBTs through the interface board.

The total dc-side voltage is controlled to be 110 V by the central NPC converter, and in order to verify the proposed VBC and compare the control performances when VBC is located at different sides, two different resistors (8.5 and 11 Ω) are connected on purpose across the upper and lower capacitors, respectively, to force the unbalanced operation.

A. Steady-State Analysis

Fig. 14 demonstrates the steady-state voltage balancing performance when VBC is located at different sides. By comparing Fig. 14(a) and (b), it can be seen that when VBC is performed at the NPC converter side, the undesirable even-order harmonics (especially second and fourth) appear at the grid-side currents

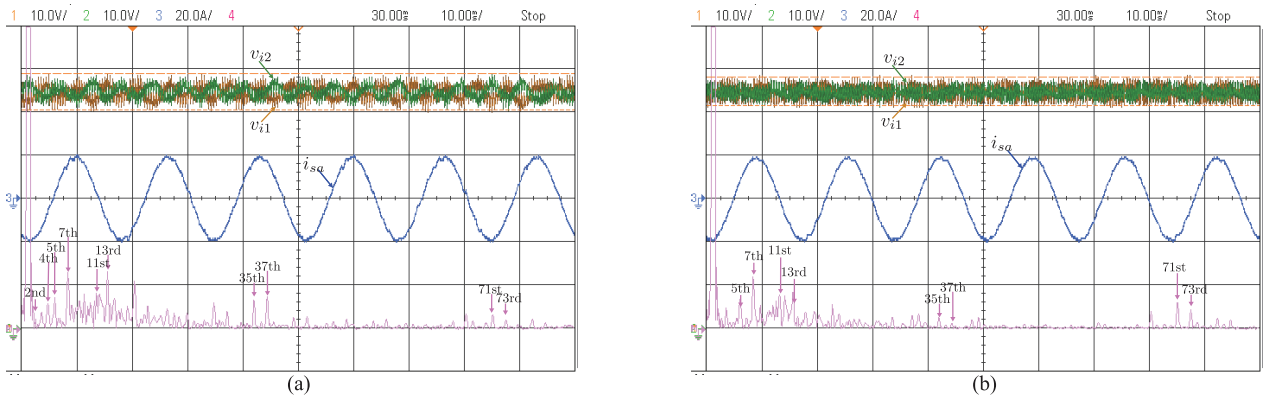

Fig. 14. Experimental steady-state performance comparison for VBC at different sides. Ch1: upper capacitor voltage v_{i1} (10 V/div). Ch2: lower capacitor voltage v_{i2} (10 V/div). Ch3: grid-side current i_{sa} (20 A/div). Math: FFT analysis of grid-side current (frequency scale: 500 Hz/div). Time scale: 10 ms/div. (a) VBC at NPC converter side. (b) VBC at TL dc–dc converter side.

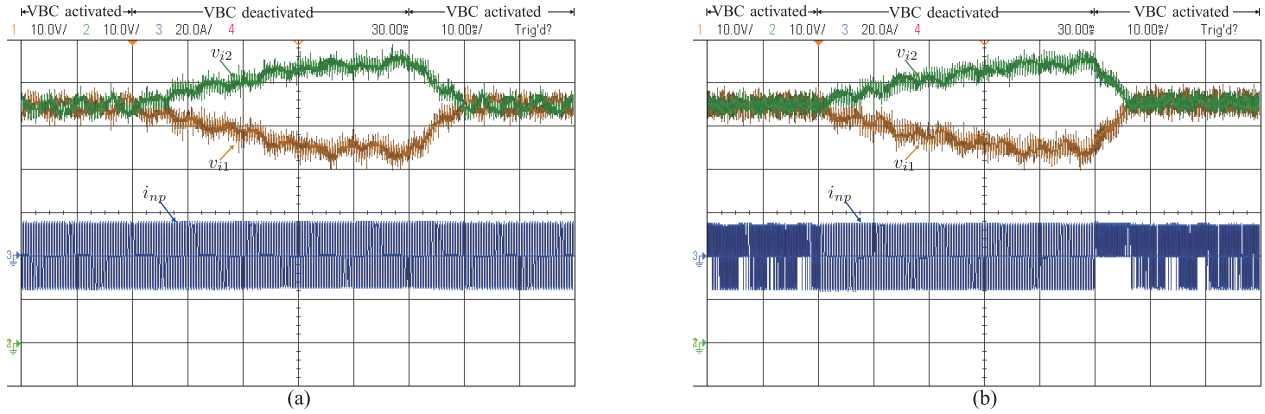

Fig. 15. Experimental disturbance performance comparison for VBC at different sides. Ch1: upper capacitor voltage v_{i1} (10 V/div). Ch2: lower capacitor voltage v_{i2} (10 V/div). Ch3: neutral-point current of TL dc–dc converter i_{np} (20 A/div). Time scale: 10 ms/div. (a) VBC at NPC converter side. (b) VBC at TL dc–dc converter side.

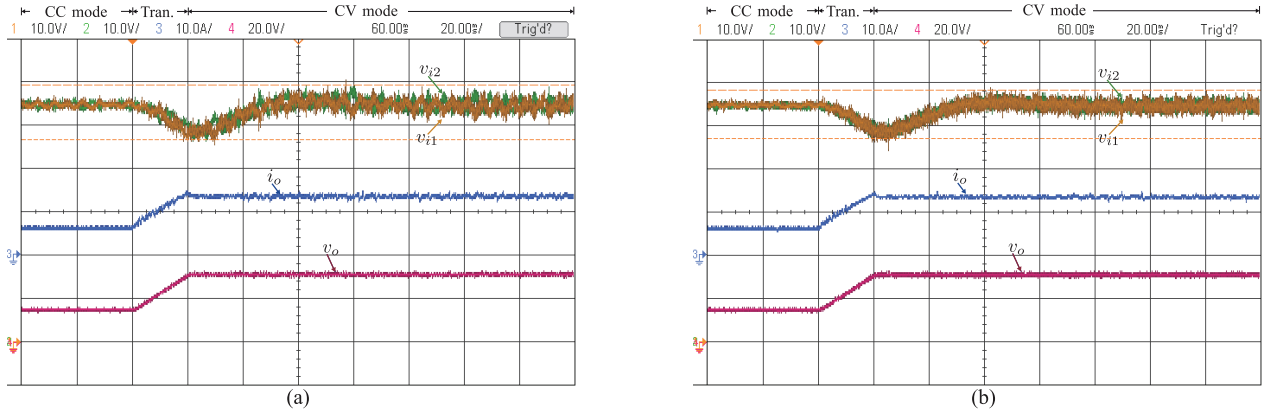

Fig. 16. Experimental transient performance comparison for VBC at different sides. Ch1: upper capacitor voltage v_{i1} (10 V/div). Ch2: lower capacitor voltage v_{i2} (10 V/div). Ch3: output current i_o (10 A/div). Ch4: output voltage v_o (20 V/div). Time scale: 20 ms/div. (a) VBC at NPC converter side. (b)VBC at TL dc–dc converter side.

and the low-frequency fluctuations appear in the dc-bus voltages. On the contrary, when VBC is performed at the TL dc–dc converter side, there is no presence of even-order harmonics in the grid-side currents, the low-frequency voltage fluctuations are suppressed, and the peak-to-peak voltage ripples are decreased from 8.7 to 7 V. It confirms that allocating VBC at TL dc–dc converter side brings benefits to the grid-side current quality and the dc-bus voltages. These results are consistent with the simulation results given in Fig. 10.

B. Disturbance Response

Fig. 15 shows the disturbance response when VBC is reactivated after its preceding deactivation. Fig. 15(b) validates

TABLE III
PERFORMANCE COMPARISON BETWEEN DIFFERENT VBC ALLOCATIONS

Comparison aspects	VBC at NPC side	Coordinated VBC
Balancing region	Limited	All covered
Balancing circuits	Needed	Not needed
Balancing response	Good	Faster
Balancing quality	Good	Excellent
Power quality	Good	Excellent

the proposed VBC performance for the TL dc–dc converter, as the two capacitor voltages converge with less settling time when VBC is reactivated, which response is faster than the one when VBC is located at the NPC converter side, as shown in Fig. 15(a). Similar to the simulation results shown in Fig. 11, Fig. 15(b) indicates that the neutral-point current i_{np} of TL dc–dc converter reaches its maximum achievable value to balance the capacitor voltages after the reactivation.

C. Transient Analysis

To continue the analysis, the transient response is provided in Fig. 16. This figure presents the VBC transient performance when fast charger is operating during the transition from CC charging mode ($i_o^* = 6\ A$) to CV charging mode ($v_o^* = 30\ V$). It shows that the output current i_o and the output voltage v_o track their references with zero steady-state error, and the transition between the two modes is smooth. The capacitor voltages are balanced during the transition process when VBC is located at different sides, but when comparing Fig. 16(a)(i) and (b)(i), it can be found that the balancing performance is improved when VBC is located at TL dc–dc converter side, as the two capacitor voltages exhibit reduced ripples and no evident low-frequency components.

VII. CONCLUSION

This paper has proposed an effective VBC together with a new modulation for high-power TL dc–dc converter-based fast charger, aiming the bipolar-dc-bus-fed EV charging station infrastructure. Fast chargers with the proposed VBC assist the NPC converter-based charging station in balancing the dc-bus voltages. The voltage balance limits of both the TL dc–dc converter and the NPC converter are explored. The VBC coordination principle between them is analyzed, and the system control diagram for the whole charging station is proposed. The steady-state analysis, the disturbance response, and the transient performance are investigated through simulation and experimental results, and compared when VBC is located at different sides.

A detailed comparison in Table III demonstrates that the proposed coordinated VBC has better performances than the one when VBC is only located at the NPC converter side. By the proposed VBC, faster balancing response is obtained as it uses the maximum available output current to balance the dc-bus voltages. Through the proposed VBC coordination, the controllable balancing region is extended from limited regions to all operating regions, so additional balancing circuits are not needed anymore, leading to reduced cost and higher efficiency. The coordinated VBC also offers better power quality and higher voltage balancing performance as it brings more freedom to the grid-side current control and removes the low-frequency fluctuations in the dc-bus voltages.

REFERENCES

[1] M. Hajian, H. Zareipour, and W. D. Rosehart, "Environmental benefits of plug-in hybrid electric vehicles: The case of Alberta," in *Proc. IEEE Power Energy Soc. Gen. Meeting*, 2009, pp. 1–6.

[2] L. Dickerman and J. Harrison, "A new car, a new grid," *IEEE Power Energy Mag.*, vol. 8, no. 2, pp. 55–61, Mar./Apr. 2010.

[3] S. G. Wirasingha and A. Emadi, "Classification and review of control strategies for plug-in hybrid electric vehicles," *IEEE Trans. Veh. Technol.*, vol. 60, no. 1, pp. 111–122, Jan. 2011.

[4] A. Emadi, L. Young-Joo, and K. Rajashekara, "Power electronics and motor drives in electric, hybrid electric, and plug-in hybrid electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2237–2245, Jun. 2008.

[5] A. S. Charles Botsford, "Fast charging vs. slow charging pros and cons for the new age of electric vehicles," in *Proc. 24th Elect. Veh. Symp.*, 2009, p. 9.

[6] B. Sanzhong and S. M. Lukic, "Unified active filter and energy storage system for an MW electric vehicle charging station," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5793–5803, Dec. 2013.

[7] S. Rivera, W. Bin, S. Kouro, V. Yaramasu, and W. Jiacheng, "Electric vehicle charging station using a neutral point clamped converter with bipolar dc bus," *IEEE Trans. Ind. Electron.*, vol. 62, no. 4, pp. 1999–2009, Apr. 2015.

[8] B. Sanzhong and S. Lukic, "Design considerations for dc charging station for plug-in vehicles," in *Proc. IEEE Veh. Power Propul. Conf. (VPPC)*, 2011, pp. 1–6.

[9] A. Kwasinski, "Quantitative evaluation of dc microgrids availability: Effects of system architecture and converter topology design choices," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 835–851, Mar. 2011.

[10] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 242–249, Mar. 2000.

[11] S. International, "SAE charging configurations and ratings terminology," SAE International, SAE Hybrid Committee Rep. 031611v18, p. 1, 2011.

[12] S. Dusmez, A. Cook, and A. Khaligh, "Comprehensive analysis of high quality power converters for level 3 off-board chargers," in *Proc. IEEE Veh. Power Propul. Conf. (VPPC)*, 2011, pp. 1–10.

[13] M. Yilmaz and P. T. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2151–2169, May 2013.

[14] A. Khaligh and S. Dusmez, "Comprehensive topological analysis of conductive and inductive charging solutions for plug-in electric vehicles," *IEEE Trans. Veh. Technol.*, vol. 61, no. 8, pp. 3475–3489, Oct. 2012.

[15] K. Taewon, K. Changwoo, S. Yongsug, P. Hyeoncheol, K. Byungik, and K. Daegyun, "A design and control of bi-directional non-isolated dc-dc converter for rapid electric vehicle charging system," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2012, pp. 14–21.

[16] C. Younghoon, A. Koran, H. Miwa, B. York, and L. Jih-Sheng, "An active current reconstruction and balancing strategy with dc-link current sensing for a multi-phase coupled-inductor converter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1697–1705, Apr. 2012.

[17] H. N. Nagaraja, D. K. Kastha, and A. Petra, "Design principles of a symmetrically coupled inductor structure for multiphase synchronous buck converters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 3, pp. 988–997, Mar. 2011.

[18] J. M. Blanes, R. Gutierrez, A. Garrigos, J. L. Lizan, and J. M. Cuadrado, "Electric vehicle battery life extension using ultracapacitors and an FPGA controlled interleaved buck-boost converter," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5940–5948, Dec. 2013.

[19] C. Woo-Young, Y. Min-Kwon, and C. Hyoung-Sup, "High-frequency-link soft-switching PWM dc-dc converter for EV on-board battery chargers," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4136–4145, Aug. 2014.
[20] Y. Min-Kwon, C. Hyoung-Sup, L. Seung-Jae, and C. Woo-Young, "High-efficiency soft-switching PWM dc-dc converter for electric vehicle battery chargers," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, 2013, pp. 1092–1095.
[21] D. Yu, S. M. Lukic, B. S. Jacobson, and A. Q. Huang, "Modulation technique to reverse power flow for the isolated series resonant dc-dc converter with clamped capacitor voltage," *IEEE Trans. Ind. Electron.*, vol. 59, no. 12, pp. 4617–4628, Dec. 2012.
[22] R. M. Cuzner, A. R. Bendre, P. J. Faill, and B. Semenov, "Implementation of a non-isolated three level dc/dc converter suitable for high power systems," in *Proc. 42nd IEEE IAS Annu. Meeting*, 2007, pp. 2001–2008.
[23] P. J. Grbovic, P. Delarue, P. Le Moigne, and P. Bartholomeus, "A bidirectional three-level dc-dc converter for the ultracapacitor applications," *IEEE Trans. Power Electron.*, vol. 57, no. 10, pp. 3415–3430, Oct. 2010.
[24] P. J. Grbovic, P. Delarue, P. Le Moigne, and P. Bartholomeus, "The ultracapacitor-based regenerative controlled electric drives with power-smoothing capability," *IEEE Trans. Ind. Electron.*, vol. 59, no. 12, pp. 4511–4522, Dec. 2012.
[25] V. Yaramasu and W. Bin, "Predictive control of a three-level boost converter and an NPC inverter for high-power PMSG-based medium voltage wind energy conversion systems," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5308–5322, Oct. 2014.
[26] S. Dusmez, A. Hasanzadeh, and A. Khaligh, "Comparative analysis of bidirectional three-level dc-dc converter for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 3305–3315, May 2015.
[27] L. Tan, B. Wu, S. Rivera, and V. Yaramasu, "Comprehensive dc power balance management in high-power three-level dc-dc converter for electric vehicle fast charging," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 89–100, Jan. 2016.
[28] D. Yu, Z. Xiaohu, B. Sanzhong, S. Lukic, and A. Huang, "Review of non-isolated bi-directional dc-dc converters for plug-in hybrid electric vehicle charge station application at municipal parking decks," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2010, pp. 1145–1151.
[29] G. R. Walker, "Digitally-implemented naturally sampled PWM suitable for multilevel converter control," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1322–1329, Nov. 2003.
[30] Y. Dongsheng, R. Xinbo, and W. Heng, "A real-time computation method with dual sampling mode to improve the current control performance of the LCL-type grid-connected inverter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4563–4572, Jul. 2015.
[31] M. Kumar and R. Gupta, "Time-domain analysis of sampling effect in DPWM of dc-dc converters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6915–6924, Nov. 2015.
[32] B. Wu, *High-Power Converters and AC Drives*. Piscataway, NJ, USA: IEEE Press, 2006.
[33] M. Malinowski, M. P. Kazmierkowski, and A. M. Trzynadlowski, "A comparative study of control techniques for PWM rectifiers in ac adjustable speed drives," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1390–1396, Nov. 2003.
[34] J. Pou, R. Pindado, D. Boroyevich, and P. Rodriguez, "Limits of the neutral-point balance in back-to-back-connected three-level converters," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 722–731, May 2004.

Longcheng Tan received the B.Eng. degree in electrical engineering from Beijing Institute of Petrochemical Technology, Beijing, China, in 2004, and the Ph.D. degree in power electronics and power drives from the Institute of Electrical Engineering, Chinese Academy of Sciences (IEECAS), Beijing, China, in 2009.

He was with the Power Electronics and Electrical Drives Research Center, IEECAS, from 2009 to 2014, where he became an Associate Professor in 2012. Currently, he is a Postdoctoral Fellow with the Laboratory for Electric Drive Applications and Research (LEDAR) and Center for Urban Energy (CUE), Ryerson University, Toronto, ON, Canada. His research interests include high-power converters, power quality, motor drives, and electric vehicles.

Bin Wu (S'89–M'92–SM'99–F'08) received the M.A.Sc. and Ph.D. degrees in electrical and computer engineering from the University of Toronto, Toronto, ON, Canada, in 1989 and 1993, respectively.

In 1993, he joined Ryerson University, Toronto, ON, Canada, where he is currently a Professor and Senior NSERC/Rockwell Automation Industrial Research Chair of Power Electronics and Electric Drives. He has authored more than 300 technical papers, authored/coauthored two Wiley-IEEE Press books, and holds more than 25 issued/pending patents in the areas of power conversion, medium-voltage drives, and renewable energy systems.

Dr. Wu is a Fellow of the Engineering Institute of Canada and Canadian Academy of Engineering (CAE). He was the recipient of the Gold Medal of the Governor General of Canada in 1993, the Premier's Research Excellence Award in 2001, the NSERC Synergy Award for Innovation in 2002, the Ryerson Distinguished Scholar Award in 2003, the YSGS Outstanding Contribution to Graduate Education Award, and the Professional Engineers Ontario Engineering Excellence Medal in 2014.

Venkata Yaramasu (S'08–M'14) received the B.Tech. degree in electrical and electronics engineering from Jawaharlal Nehru Technological University, Hyderabad, Hyderabad, India, in 2005, the M.E. degree in electrical engineering with specialization in power electronics from Shri Govindram Seksaria Institute of Technology and Science, Indore, India, in 2008, and the Ph.D. degree in electrical engineering from Ryerson University, Toronto, ON, Canada, in 2014.

From 2014 to 2015, he was a Postdoctoral Research Fellow with the Laboratory for Electric Drive Applications and Research (LEDAR) and Center for Urban Energy (CUE), Ryerson University. He is currently an Assistant Professor with the Department of Electrical Engineering and Computer Science, Northern Arizona University, Flagstaff, AZ, USA. His research interests include high-power converters, electric drives, renewable energy, electric vehicles, and model predictive control.

Sebastian Rivera (S'10–M'16) was born in Valparaiso, Chile, in 1986. He received the B.Sc. and M.Sc. degrees in electronics engineering from the Universidad Tecnica Federico Santa Maria (UTFSM), Valparaiso, Chile, in 2007 and 2011, respectively, and the Ph.D. degree in electrical and computer engineering from Ryerson University, Toronto, ON, Canada, in 2015. His research interests include multilevel converters, renewable energy conversion systems, and electric vehicles.

Dr. Rivera was the recipient of the Emerging Leaders in the Americas Program Scholarship from the Canadian Bureau for International Education in 2010 and the Ph.D. Scholarship from the Chilean National Commission for Scientific and Technological Research (CONICYT).

Xiaoqiang Guo (M'10–SM'14) received the B.S. and Ph.D. degrees in electrical engineering from Yanshan University, Qinhuangdao, China, in 2003 and 2009, respectively.

He was a Postdoctoral Fellow with the Laboratory for Electrical Drive Applications and Research (LEDAR), Ryerson University, Toronto, ON, Canada. He is currently an Associate Professor with the Department of Electrical Engineering, Yanshan University. He has authored/coauthored more than 50 technical papers, in addition to 9 patents. His research interests include high-power converters and ac drives, electric vehicle charging stations, and renewable energy power conversion systems.