Comprehensive DC Power Balance Management in High-Power Three-Level DC–DC Converter for Electric Vehicle Fast Charging

Longcheng Tan, *Member, IEEE*, Bin Wu, *Fellow, IEEE*, Sebastian Rivera, *Student Member, IEEE*, and Venkata Yaramasu, *Member, IEEE*

***Abstract*—With the increasing popularity of electric vehicles, there is an urgent demand to shorten the charging time, so the development of high-power charging stations with fast chargers is necessary to alleviate range anxiety for drivers. The charging station based on the neutral-point-clamped (NPC) converter can bring many merits, but it has unbalanced power problems in the bipolar dc bus. To solve this issue, comprehensive dc power balance management (PBM) in conjunction with high-power three-level dc–dc converter based fast charger is proposed in this paper. The active dc power balance management (APBM) is proposed to assist the central NPC converter in balancing power so that the additional balancing circuit is eliminated; while the passive dc power balance management (PPBM) is proposed to eliminate the fluctuating neutral-point currents and to ensure the balanced operation of fast chargers. The principles of APBM and PPBM are researched, the efficient integration between them is studied, and the overall control scheme for the fast charger is proposed. The power balance limits of APBM are explored, while the circulating currents of PPBM are analyzed. Simulation and experimental results are presented to verify the effectiveness of the proposed fast charger with PBM functions.**

***Index Terms*—Dc power balance management, electric vehicles, fast charger, plug-in hybrid electric vehicles, three-level dc–dc converter.**

I. Introduction

As viable alternatives to conventional internal combustion engine vehicles (ICEVs), the plug-in hybrid electric vehicles and electric vehicles (EVs) are increasing their market share gradually because of decreased fossil fuels consumption and reduced greenhouse gas emission [1], [2]. Surveys show that the range per charge, the charging time, the available charging facilities are the greatest concerns of consumers, which are also the main factors influencing their purchase of EVs [3], [4]. In order to allow the future widespread use of EVs, there is an urgent demand to develop fast chargers to shorten the charging time, and to deploy the high-power charging stations infrastructure to alleviate range anxiety for drivers. If fast chargers reduce the EVs replenishing time within acceptable levels comparable to the usual refueling of ICEVs, and the high-power charging stations spread all over the cities and highways as the gas stations do, the acceptance of EVs will be enhanced [1]–[5].

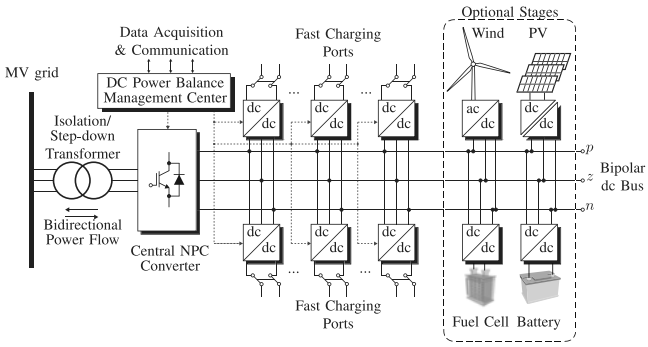

Fig. 1. Bipolar dc bus charging station architecture [6].

The high-power charging station architectures include two main groups: One uses common ac bus, the other uses common dc bus, but the latter seems a preferable one as less conversion stages are needed so that higher system efficiency can be obtained, and it is easier to integrate the storage systems (batteries or ultra-capacitors) and the renewable energy sources (the photovoltaic and wind) [5], [6]. The common dc-bus architecture can be realized as unipolar dc bus using two-level voltage source converters or bipolar dc bus using three-level neutral-point-clamped (NPC) converters. The bipolar dc bus architecture has been previously analyzed in [6] using an NPC converter as the central grid-tied ac–dc converter. The bipolar dc architecture as shown in Fig. 1 offers more power capacity, more flexible ways for the loads to be connected to the dc bus. Moreover, the line-to-line voltage waveform of the two-level voltage source converter contains three voltage levels, whereas the NPC converter produces five voltage levels and the equivalent switching frequency of the NPC converter is twice the device switching frequency, leading to lower dv/dt, lower filtering requirement, and better current performance [7]–[11]. However, the configuration in [6] suffers from imbalanced power between the positive dc bus and the negative dc bus, because each dc bus is independent and their loads differ most of the time. The imbalanced power can lead to worse grid-side currents and make the bipolar dc bus unbalanced, even outside of the controllable zone. In order to solve this problem, the study in [6] introduced an

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The authors are with the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON M5B 2K3, Canada (e-mail: ltan@ee.ryerson.ca; bwu@ee.ryerson.ca; srivera@ee.ryerson.ca; vyaramas@ee.ryerson.ca).

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additional balancing circuit, but with the drawbacks of additional cost and poorer efficiency.

In addition to the central charging station architecture, the dc–dc converters employed in the fast chargers also play a crucial role on the system efficiency and battery charging time. The level I and II chargers are usually employed for slow charging, and the power rating of them is low, thus they are usually mounted on-board [12]–[14]. Comparatively, in order to shorten the charging time, the voltage level and power rating of fast chargers (dc level III) are much higher, usually with dc voltage from 200 to 600 V and power rating from 50 to 240 kW [12], [15], so it must be integrated with the off-board central charging stations. The electrical isolation between the electric grid and battery packs can be provided by the central charging station or fast chargers. The studies in [15]–[19] introduced isolated soft-switching dc–dc converters to perform fast charging with electrical isolation. Since the central high-power charging station usually includes an isolation transformer, the dc–dc converters employed in fast chargers do not need to provide electrical isolation, so high-power nonisolated dc–dc converters are most suitable and economical candidates [20].

The multiphase interleaved buck converters have been discussed in [21]–[25] to share the high charging power between multiple modules, but they are more suitable for integration with the charging station based on two-level voltage source converters due to the voltage matching. The three-level dc–dc converters have been applied in power factor correction [26], renewable energy systems [27], [28], fuel-cell applications [29], [30], and storage systems [30]–[32] to achieve high-voltage, high-power rating and to reduce the output filter size compared to the two-level dc–dc converters. These applications were mainly for unidirectional power flow, and few of them researched on the dc power balance management in the charging station field. However, EVs charging infrastructure requires bidirectional dc–dc converters to facilitate the vehicle-to-grid (V2G) and grid-to-vehicle (G2V) operation [33]. Meanwhile, when the charging station with a bipolar dc bus based on the NPC converter is chosen, the nature of this application cannot guarantee a balanced power between the bipolar bus loads, as the charging ports are used randomly with the arrival of the EVs. Unbalanced power leads to unbalanced voltage, resulting in poor current performance and even damage to the equipment, therefore the presence of a dc power balance management mechanism is mandatory.

This paper proposes comprehensive dc power balance management in conjunction with high-power three-level dc–dc converter based fast chargers for high-power charging stations with a bipolar dc bus. The proposed fast charger with dc power balance management capability eliminates the need for additional balancing circuits and high-frequency transformers, thereby improves the overall system efficiency. Meanwhile, since the dc power balance management task is partly achieved by the three-level dc–dc converters, the central NPC converter has more freedom to accurately control the grid-side currents leading to higher power quality. To solve the unbalanced dc power problem among the positive dc bus and the negative dc bus, the comprehensive dc power balance management is proposed. The active and passive dc power balance managements (APBM and PPBM) are investigated from the aspects of operating principles, balance limits and circulating currents. The efficient integration between APBM and PPBM is studied, and the overall control scheme for the fast charger is proposed. The performance of the proposed fast charger and control algorithms are verified through simulation and experimental results.

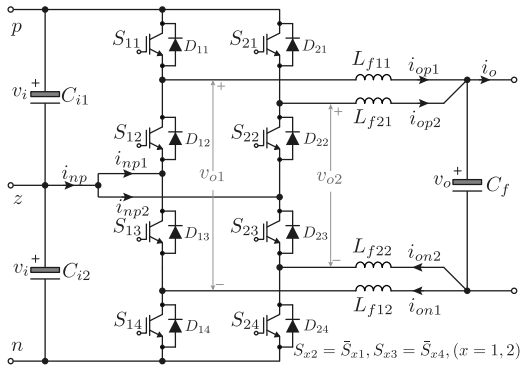

Fig. 2. Proposed three-level dc–dc converter topology.

II. High-Power Three-Level DC–DC Converter

A. Topology Description

The structure of the proposed converter for high-power fast chargers is presented in Fig. 2. It consists of two parallel three-level dc–dc converter units to handle the high charging current, and the input terminals p, z, n directly fit the bipolar dc bus of the central charging station shown in Fig. 1. Each unit is composed of four switching devices along with four freewheeling diodes, and two output inductors. The nomenclature of each component is shown in Fig. 2. The converter structure is modular in nature because the parallel dc–dc converters share common input filter capacitors C_{i1}, C_{i2}, and common output filter capacitor C_f, so the power capacity can be easily scaled up by connecting more number of dc–dc converters in parallel.

B. Modulation and Operating Principle

The modulation method and operating principle of the proposed fast charger is presented in Fig. 3, for the case when the system is under balanced power conditions and the two converter units operate in the in-phase mode (with their gating signals having no phase difference). Under this mode, the instantaneous power sharing of the proposed dc–dc converter is always equal, which is different from the interleaved converters [21], [22], [34], [35]. Two operating regions are presented to analyze the converter. Fig. 3(a) shows the converter waveforms when $d_{x1}{=}d_{x4}{=}d \leq 0.5$, and Fig. 3(b) shows the waveforms when $d_{x1}{=}d_{x4}{=}d > 0.5$. The modulation signals d_{x1} and d_{x4} are duty cycles generated by the controller, where x denotes 1 or 2 corresponding to unit 1 or unit 2.

As shown in Fig. 3, the modulation signals (duty cycle values) d_{x1} and d_{x4} are compared with two 180° interleaved carrier signals c_1, c_4 to generate the gate signals for outer switches S_{x1} and S_{x4}, while the inner switches S_{x2} and S_{x3} operate complementarily to their corresponding adjacent outer switches,

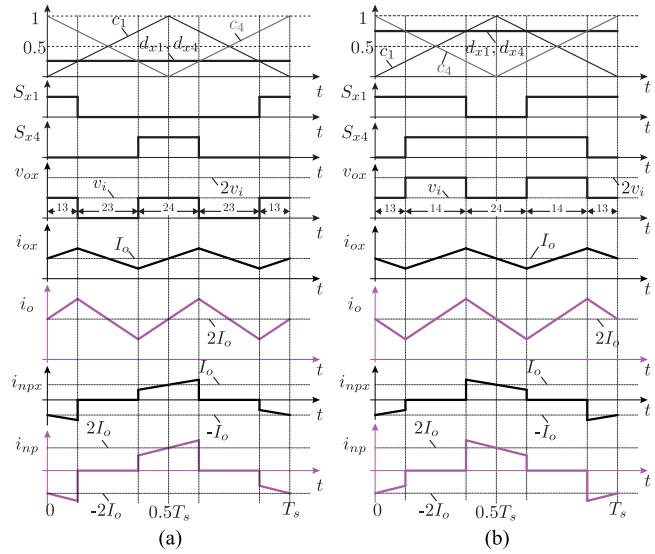

Fig. 3. Modulation and operating principle. (a) $d \leq 0.5$. (b) $d > 0.5$.

respectively. This leads to four operating stages: 14, 13, 23 and 24, where the numbers denote which switches are turned ON. The output voltage of stage 14 is the total dc side voltage $2v_i$; the stage 23 produces zero output voltage; while the stages 13 and 24 generate the same output voltage v_i but have opposite neutral-point currents, which enables the converter to have the dc power balance management capability.

From Fig. 3, it can be found that the generated voltages v_{o1} and v_{o2} of each unit oscillate between 0 and v_i for $d \leq 0.5$ (there are only transitions among stages 13, 23 and 24); on the contrary, these voltages change between v_i and $2v_i$ for $d > 0.5$ (the switching stages transit among 13, 14 and 24). This leads to the output voltages with three voltage levels 0, v_i and $2v_i$. Based on the aforementioned analysis and Fig. 3, the output currents of each unit can be formulated in (1). Because all the unit output currents i_{op1}, i_{on1}, i_{op2} and i_{on2} have the same formula under the in-phase mode, they are denoted as i_{ox}.

$$i_{ox}(t) = \begin{cases} I_o + \dfrac{\Delta i_{ox}}{dT_s} t, & \dfrac{kT_s}{2} \leq t \leq \dfrac{(k+d)T_s}{2} \\ I_o - \dfrac{\Delta i_{ox}\,(4t - T_s)}{2(1-2d)T_s}, & \dfrac{(k+d)T_s}{2} \leq t \leq \dfrac{(k+1-d)T_s}{2} \\ I_o + \dfrac{\Delta i_{ox}}{2dT_s}\,(2t - T_s), & \dfrac{(k+1-d)T_s}{2} \leq t \leq \dfrac{(k+1)T_s}{2} \end{cases} \quad (1)$$

where T_s is the switching period, k is a positive integer ($k \in [0, +\infty)$), I_o is the average output current of each unit and Δi_{ox} is the output current ripple of each unit, which can be modeled as

$$\Delta i_{ox} = \begin{cases} d(1-2d)T_s v_i / L_f, & d \leq 0.5 \\ (1-d)(2d-1)T_s v_i / L_f, & d > 0.5 \end{cases} \quad (2)$$

where $L_f = L_{fx1} + L_{fx2} = 2L_{fx1}$ denotes the total output inductance of each unit. As shown in Fig. 3, the equivalent frequency of the output quantities i_{ox}, i_o and v_{ox} is two times the device switching frequency, hence the requirements for output inductive and capacitive filters can be reduced [31].

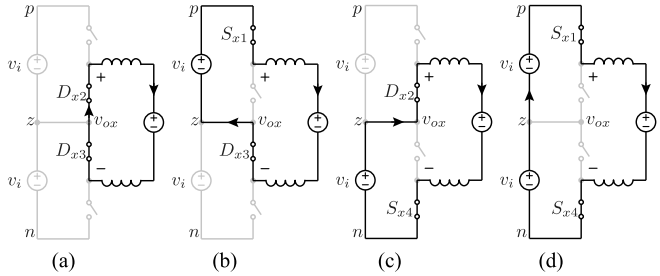

Fig. 4. Four operating stages and their equivalent circuits. (a) 23. (b) 13. (c) 24. (d) 14.

III. Active DC Power Balance Management (APBM)

A. APBM Principle

Because there are inherent balance limits of the central NPC converter (refer to Fig. 1) [6], [9], in order to assist it in balancing power between the dc buses and remove the additional balancing circuit, APBM for fast chargers is proposed. Under the APBM mode, the fast chargers can perform the power balance task actively so that the central NPC converter has more freedom to control the grid-side currents, resulting in better power quality.

To simplify the analysis, it is assumed that the split dc-link capacitor voltages are balanced and equal to v_i, the output current polarity is positive (G2V operation), and the output filter capacitor along with the battery load is replaced by an ideal voltage source, then the equivalent circuits of the four operating stages (23, 13, 24, 14) are shown in Fig. 4. It can be seen that operating stages 23 and 14 do not have impact on power balance, as there is no current flowing through the neutral point z, while switching stages 13 and 24 have the opposite impact on the power balance: Stage 13 draws power from the positive dc bus while stage 24 draws power from the negative dc bus. Therefore, based on this feature, the APBM principle can be formulated: For a charging station, if the power on the positive dc side P_p is lower than the power on the negative dc side P_n, it is necessary to make the dwell time for state 13 longer while the time for state 24 has to be shorter, so that the fast charger draws more power from the positive bus to aid the charging station to balance power. On the contrary, if P_p is larger than P_n the opposite regulation needs to be done, that is, time for stage 13 should be reduced while time for stage 24 should be increased.

Fig. 5 shows the APBM principle explicitly only considering $d > 0.5$ and the positive output current, however is also valid for $d \leq 0.5$. Under balanced power conditions, the modulation indexes d_{x1} and d_{x4} are both equal to d, but under the presence of unbalances they must be regulated to different values accordingly. Compared to the balanced scenario (shown by black line) where $d_{x1} = d_{x4} = d$ and the average value of i_{npx} is zero, when $P_p < P_n$, the dwell time for stage 24 is decreased while time for stage 13 is increased as shown in the shaded area of Fig. 5(a), leading to $d_{x1} > d_{x4}$ (shown by blue line) and the negative average value of i_{npx}. However, the average value of output voltage v_{ox} remains unchanged. The opposite situation

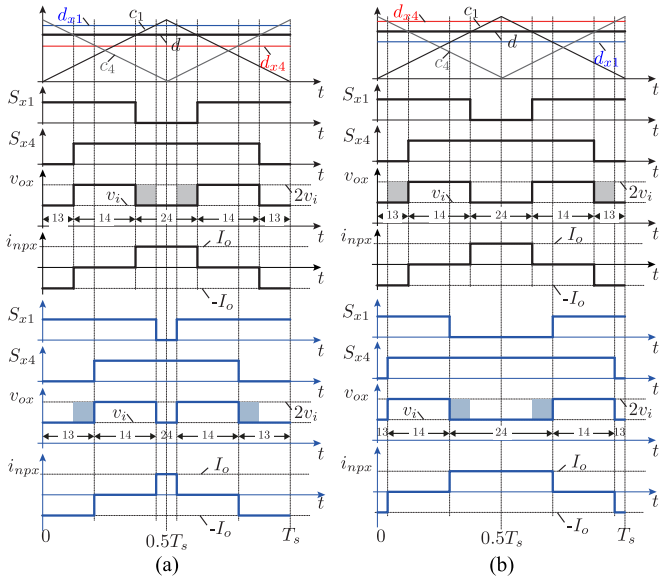

Fig. 5. APBM principle. (a) $d_{x1} > d_{x4}$. (b) $d_{x1} < d_{x4}$.

is shown in Fig. 5(b), where $P_p > P_n$ as the dwell time for stage 24 is increased while time for stage 13 is decreased, resulting in $d_{x1} < d_{x4}$ and the positive average value of i_{npx}. Aforementioned analysis is based on the assumption that the output current is positive, but when the output current is negative (V2G operation), the regulation process should be done inversely.

B. Power Balance Limits of APBM

In order to allocate power balance tasks among the operating fast chargers and the central NPC converter efficiently, it is important to explore the power balance limits of APBM for the fast chargers, especially the balance power it can provide under different operating conditions.

Using the operating principles presented earlier in Figs. 3 and 5, the maximum average value of total neutral-point current i_{np} is calculated

$$\hat{I}_b = \begin{cases} 4dI_o, & d \le 0.5 \\ 4(1-d)I_o, & d > 0.5 \end{cases} \tag{3}$$

where I_o is the average output current of each unit. Then, the corresponding maximum balance power $\hat{P}_b$ of the converter is

$$\hat{P}_b = \begin{cases} P_o, & d \le 0.5 \\ (1/d-1)P_o, & d > 0.5 \end{cases} \tag{4}$$

where P_o is the total output power, so the power ratio η between the maximum balance power $\hat{P}_b$ and the total output power P_o is

$$\eta = \begin{cases} 1, & d \le 0.5 \\ 1/d-1, & d > 0.5. \end{cases} \tag{5}$$

The power balance limits of APBM are plotted in Fig. 6. The shaded area is the balance power which can be provided by the proposed converter when the duty cycle changes from 0 to 1. It can be found that the maximum balance power $\hat{P}_b$ equals to

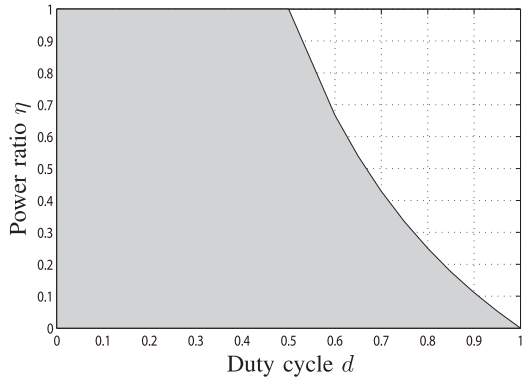

Fig. 6. Power balance limits of APBM.

the total output power P_o when $d \le 0.5$; while for $d > 0.5$, the maximum balance power $\hat{P}_b$ is inversely proportional to d.

It should be mentioned that since all the proposed fast chargers are connected to the bipolar dc bus with access to the neutral point and have their own power balance capabilities, the unbalanced power of the charging station only results from the unsymmetrical circuit parameters and practical unequal gating signals delays, etc., which is quite small and can be handled by the NPC converter, so the additional balancing circuit is not needed anymore.

IV. Passive DC Power Balance Management (PPBM)

A. PPBM Principle

Since all the three-level dc–dc converter based fast chargers have access to the neutral point of the central NPC converter as shown in Fig. 1, although the average capacitor voltages are equal under balanced operating conditions, the accumulated total neutral-point current fluctuation is drastic and leads to big voltage fluctuations at the dc-side capacitors, which is harmful to the safety and lifetime of capacitors [9]. In order to solve this problem, the PPBM is proposed. Under the PPBM mode, the proposed parallel three-level dc–dc converters feature a virtual disconnection to the neutral-point, working as the two-level converter connected to the total dc bus directly, hence minimizes the presence of the total neutral-point current and guarantees the balanced power operation of fast chargers. From the charging station point of view, if all the fast chargers are operating under the PPBM mode, there will be no unbalanced power between the dc buses, however, as the total neutral-point current is zero, it cannot balance the dc power actively, that is the reason why it is called PPBM.

As demonstrated earlier in Fig. 4, the two stages 13 and 24 produce the same output voltage magnitude but with opposite neutral-point current polarities, while states 14 and 23 do not influence the neutral-point currents. Hence, if the two dc–dc converter units operate in the out-of-phase mode (with their gating signals having 180° phase difference) as shown in Fig. 7, the neutral-point currents i_{np1}, i_{np2} will cancel each other, ideally leading to the total neutral-point current $i_{np} = 0$ while the output voltage remains unaltered. From the charging station point of view, the dc–dc converter operates like a virtual two-level

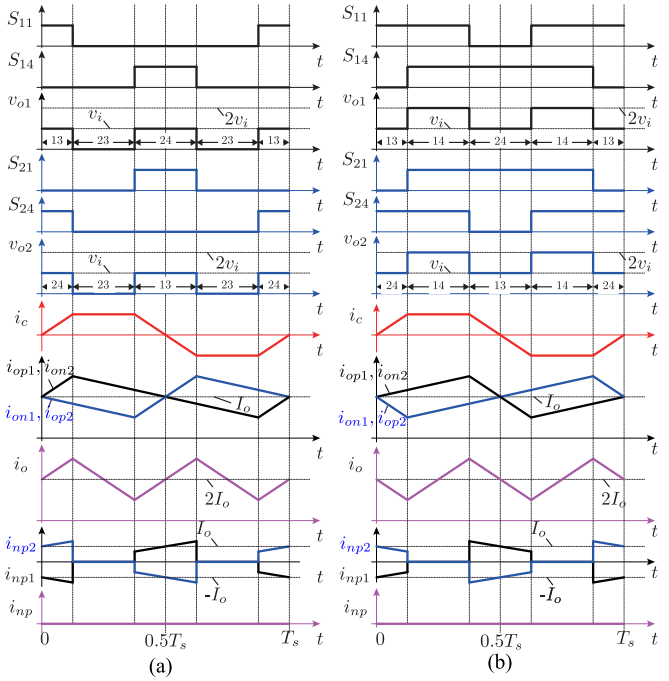

Fig. 7. PPBM principle. (a) $d \leq 0.5$. (b) $d > 0.5$.

converter because it fetches power from the total dc bus directly. Obviously, this operation is beneficial to the charging station with a bipolar dc bus, because the fast charger does not cause power imbalance problems.

When under the PPBM mode, from the gating signals point of view, the proposed operating mode is similar with the operating mode of two interleaved converters, because both of them have 180° phase difference between the gating signals. But the proposed two parallel converters receive power from different dc sides, which is still different from the power sharing of two interleaved converters [21], [22], [34], [35]. Comparing the total neutral-point current i_{np} shown in Fig. 7 with the one shown in Fig. 3, it can be found there are no fluctuant neutral-point currents under the PPBM mode. Because of this, issues related with both power and voltage fluctuations are minimized, as the presence of many fast chargers and operating simultaneously do not have a strong impact on the dc bus, leading to reduced requirements for the dc-side capacitors.

B. Circulating Currents of PPBM

When the two parallel units are in out-of-phase operation, as shown in Fig. 7, there are circulating currents between them. Fig. 8 represents the paths for the upper circulating current i_{cp} and the lower circulating current i_{cn}. The amplitudes of these circulating currents depend on the overlapped dwell time of stages 13 and 24.

Assuming $d_{x1} = d_{x4} = d$, and based on Figs. 7 and 8, the circulating current ripple Δi_c is given by

$$\Delta i_c = \begin{cases} dT_s v_i / L_f, & d \leq 0.5 \\ (1-d) T_s v_i / L_f, & d > 0.5. \end{cases} \tag{6}$$

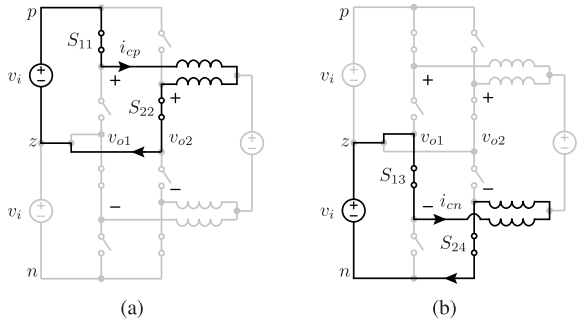

Fig. 8. Paths for the circulating currents: (a) upper circulating current i_{cp}, (b) lower circulating current i_{cn}.

Then the expressions for circulating currents i_{cp} and i_{cn} are obtained, and as these currents share the same expression, both of them are denoted as i_c, whose waveforms are shown in Fig. 7.

$$i_c(t) = \begin{cases} \dfrac{\Delta i_c}{dT_s} t, & kT_s \leq t \leq \left(k + \dfrac{d}{2}\right) T_s \\ \dfrac{\Delta i_c}{2}, & \left(k + \dfrac{d}{2}\right) T_s \leq t \leq \left(k + \dfrac{1-d}{2}\right) T_s \\ \dfrac{\Delta i_c}{2d} - \dfrac{\Delta i_c}{dT_s} t, & \left(k + \dfrac{1-d}{2}\right) T_s \leq t \leq (k + \dfrac{1+d}{2}) T_s \\ -\dfrac{\Delta i_c}{2}, & \left(k + \dfrac{1+d}{2}\right) T_s \leq t \leq \left(k + 1 - \dfrac{d}{2}\right) T_s \\ -\dfrac{\Delta i_c}{d} + \dfrac{\Delta i_c}{dT_s} t, & \left(k + 1 - \dfrac{d}{2}\right) T_s \leq t \leq (k+1) T_s. \end{cases} \tag{7}$$

From (6) and (7), it can be seen that the maximum value for i_c is $0.5 v_i T_s / L_f$ happening at $d = 0.5$; meanwhile, based on Fig. 5 and (1), the maximum ripple of the total output current under APBM is also $0.5 v_i T_s / L_f$ happening at $d = 0.25$ or 0.75. In other words, the amplitude of circulating currents is always lower than the maximum ripple of the total output current.

Moreover, by combining (1), (2) and (7), the expression for the total output current i_o of Fig. 7 can be obtained

$$i_o = 2 i_{ox} \tag{8}$$

meaning that, although the PPBM makes the unit output current ripples a little bigger due to the circulating currents, the total output current ripple remains the same as there is no PBM used under the balanced power condition.

V. Comprehensive DC Power Balance Management

Based on the proposed APBM and PPBM as discussed in the previous two sections, the comprehensive dc power balance management is formulated. When the imbalanced power between the dc buses is outside of the predefined controllable zone of the central NPC converter, the APBM is activated to assist it in balancing power so that additional balancing circuits can be eliminated; while when the imbalanced power is within its balanced zone, the PPBM is chosen to ensure the balanced operation of fast chargers and minimize the fluctuant neutral-point currents. By this way, the comprehensive dc power balance management combines the advantages of APBM and PPBM

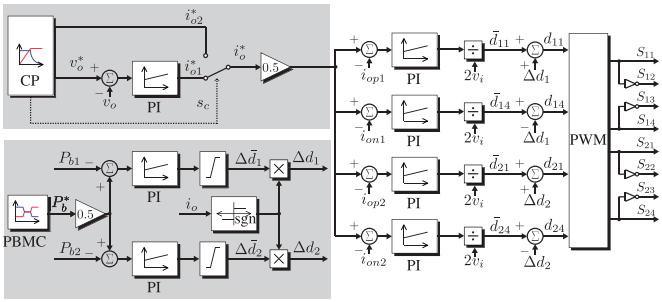

Fig. 9. Control diagram for the fast charger with comprehensive dc power balance management.

TABLE I
SIMULATION AND EXPERIMENTAL PARAMETERS

Parameter	Sym.	Sim. value	Exp. value
Total dc voltage	$2v_i$	$3.\bar{3}$ p.u.	$3.\bar{3}$ p.u.
Input capacitance	C_i	0.56 p.u.	0.56 p.u.
Output inductance	L_f	1.25 p.u.	1.25 p.u.
Output capacitance	C_f	$0.\bar{6}$ p.u.	$0.\bar{6}$ p.u.
Switching frequency	f_s	72 p.u.	72 p.u.
Base frequency	f_{B}	60 Hz	60 Hz
Base voltage	V_{B}	600 V	42 V
Base power	P_{B}	240 kW	1.2 kW

Note: Output side values are used as the base quantities.

to achieve most beneficial cooperation for the overall power balance of the charging station. Therefore, the transition between APBM and PPBM is proposed to be triggered by the power difference ΔP between P_p and P_n. When ΔP is outside of a predetermined region, the APBM is selected; when it falls into this region, the PPBM is chosen. The explicit transition rule for it is as follows:

$$\mathrm{PBM} = \begin{cases} \mathrm{APBM}, & \text{when } \Delta P \notin [-P_{b\epsilon}, P_{b\epsilon}] \\ \mathrm{PPBM}, & \text{when } \Delta P \in [-P_{b\epsilon}, P_{b\epsilon}] \end{cases} \tag{9}$$

where $P_{b\epsilon}$ is chosen based on the balance limits of the central NPC converter [6] and the balance task sharing between it and the operating fast chargers.

Then, the control scheme for the fast charger with comprehensive dc power balance management is presented in Fig. 9. The upper grey box represents the output voltage and current control, where the charging profile (CP) provides the reference current i_{o2}^*, the reference voltage v_o^*, and the switch signal s_c to control the transition between the constant current (CC) charging mode and the constant voltage (CV) charging mode. Then, as the two units share the total output current, the current reference of each unit is set to $i_o^*/2$ and the four output currents of two converter units are controlled using four PIs, then the outputs of PIs are divided by the total input voltage $2v_i$ to generate the original modulation signals $\bar{d}_{x1}, \bar{d}_{x4}$.

The lower grey box shows the comprehensive dc power balance management, where the power balance management center (PBMC) commands the required balance power reference P_b^*, which is easy for PBMC to calculate after collecting voltages and currents information from all loads connected to the bipolar dc bus of a charging station, and knowing the number of operating fast chargers n

$$P_b^* = \Delta P/n = (P_n - P_p)/n. \tag{10}$$

Meanwhile, the balance power P_{bx} generated by each converter unit can be obtained based on the Figs. 4 and 5

$$P_{bx} = (d_{x1} - d_{x4}) v_i i_{ox}. \tag{11}$$

The balance power is controlled with two PIs, generating the control signals $\Delta\bar{d}_x$, which are limited to be within the boundary $[-\Delta\hat{d}_x, \Delta\hat{d}_x]$, and $\Delta\hat{d}_x$ is defined as follows:

$$\Delta\hat{d}_x = \begin{cases} \min\{\bar{d}_{x1}, \bar{d}_{x4}\}, & \bar{d}_{x1,x4} \le 0.5 \\ 1 - \max\{\bar{d}_{x1}, \bar{d}_{x4}\}, & \bar{d}_{x1,x4} > 0.5. \end{cases} \tag{12}$$

Then, depending on the power flow direction, the power balance control signal Δd_x is finally obtained by multiplying $\Delta\bar{d}_x$ by the sign of the total output current i_o

$$\Delta d_x = \Delta\bar{d}_x \mathrm{sgn}(i_o). \tag{13}$$

After obtaining Δd_x, and using the original modulation signals $\bar{d}_{x1}, \bar{d}_{x4}$, the final modulation signals d_{x1}, d_{x4} are calculated

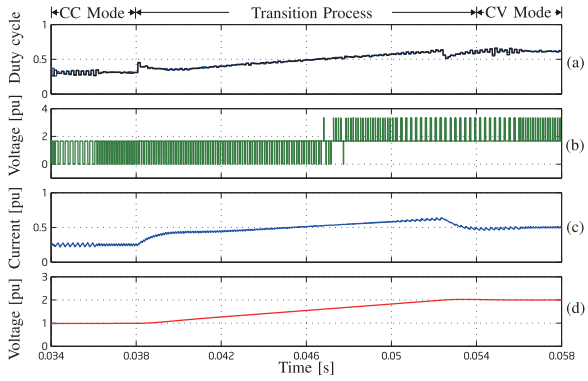

Fig. 10. Simulated results for transition from CC mode to CV mode. (a) Modulation signals d_{11} and d_{14}. (b) Unit 1 output voltage v_{o1}. (c) Total output current i_o. (d) Output voltage v_o.

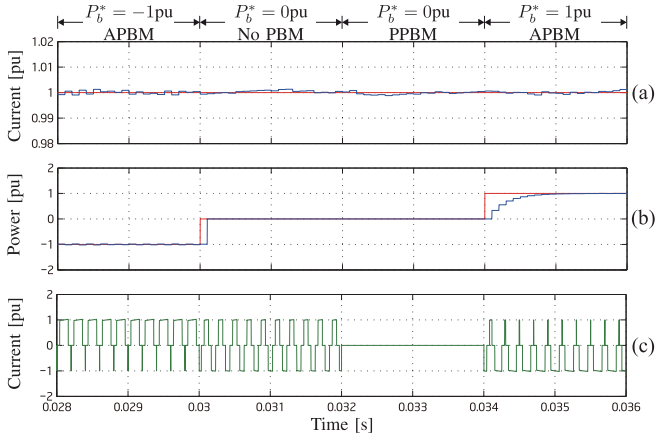

Fig. 11. Simulated dynamic performance of PBM in CC mode, for $d \le 0.5$. (a) Total output current i_o and its reference i_o^*. (b) Balance power P_b and its reference P_b^*. (c) Total neutral-point current i_{np}.

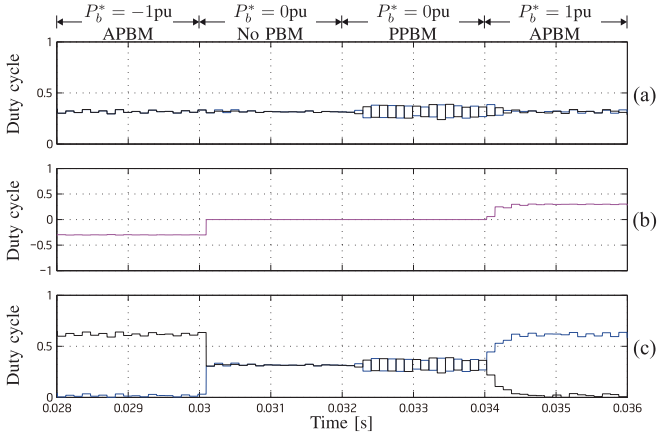

Fig. 12. Simulated dynamic performance of the modulation signals in CC mode, for $d \leq 0.5$. (a) Original modulation signals $\bar{d}_{11}$ and $\bar{d}_{14}$. (b) Power balance control signal Δd_1. (c) Final modulation signals d_{11} and d_{14}.

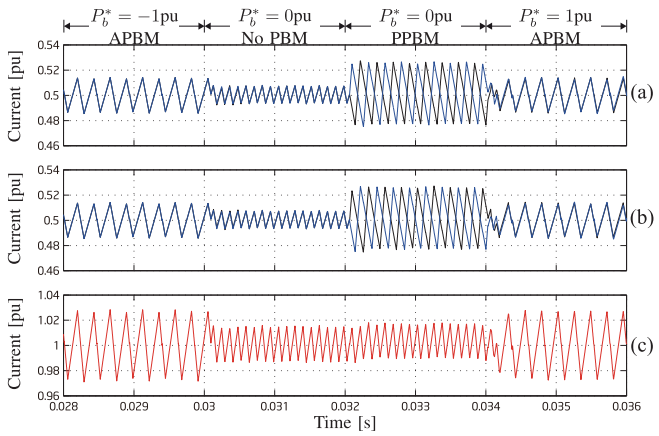

Fig. 13. Simulated dynamic performance of the output currents in CC mode, for $d \leq 0.5$. (a) Unit 1 output currents i_{op1} and $i_{\mathrm{on}1}$. (b) Unit 2 output currents i_{op2} and $i_{\mathrm{on}2}$. (c) Total output current i_o.

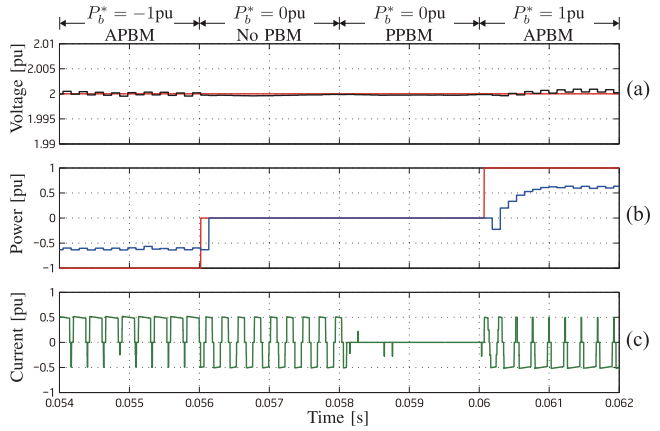

Fig. 14. Simulated dynamic performance of PBM in CV mode, for $d > 0.5$. (a) Output voltage v_o and its reference v_o^*. (b) Power balance P_b and its reference P_b^*. (c) Total neutral-point current i_{np}.

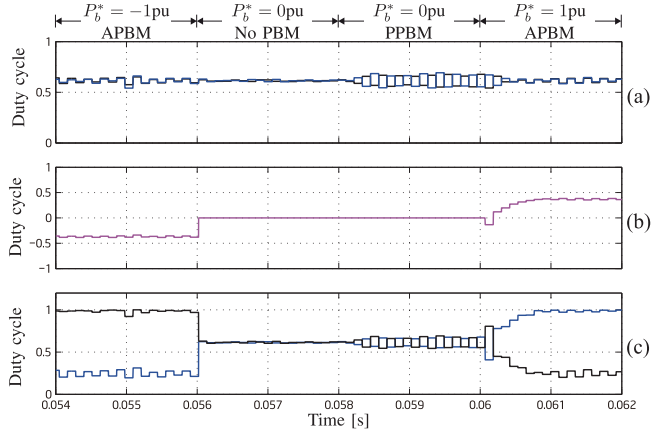

Fig. 15. Simulated dynamic performance of the modulation signals in CV mode, for $d > 0.5$. (a) original modulation signals $\bar{d}_{11}$ and $\bar{d}_{14}$. (b) Power balance control signal Δd_1. (c) final modulation signals d_{11} and d_{14}.

according to the following equations:

$$d_{x1} = \bar{d}_{x1} + \Delta d_x \tag{14}$$

$$d_{x4} = \bar{d}_{x4} - \Delta d_x. \tag{15}$$

Then the gating signals are generated through the modulation discussed in Section II-B. It should be noticed that when PPBM is chosen, the switching signals for the two units should be phase shifted 180°.

VI. Simulation Results

The proposed fast charger with comprehensive dc power balance management is simulated using MATLAB/Simulink. A 240-kW converter is designed for the validation, and the detailed system parameters are shown in Table I.

To validate the scheme, the following scenario is simulated. The converter begins operating under CC charging mode, and four scenarios are forced in order to illustrate the dc power balance management with $d \leq 0.5$. The converter begins operating in APBM with $P_b^* = -1$p.u., then in order to emphasize the features of PPBM, no PBM is performed after 0.030 s (under balanced power conditions). Then PPBM is activated at 0.034 s and then the converter is set to operate in APBM with $P_b^* = 1$p.u. Then when the system triggers the control scheme to operate under CV charging mode, the same test is performed once again now with $d > 0.5$.

The overall transition process from CC mode to CV mode is presented in Fig. 10, where it can be seen how the duty cycles change along the simulation from 0.034 to 0.058 s. In addition, Fig. 10(b) presents the generated voltage v_{o1} of unit 1, exhibiting three voltage levels on its waveform as established in the previous sections, and it becomes clear that the voltages oscillate between 0 and v_i for $d \leq 0.5$; and between v_i and $2v_i$ when $d > 0.5$.

Then, the dc power balance management under CC mode is validated through Figs. 11 to 13, where the total output current reference i_o^* is set to 1 p.u. throughout the test, while P_b^* is changed in order to validate all the operation modes as presented in Fig. 11(b). From Fig. 11, it can be seen that the total output current i_o is controlled to its reference i_o^* tightly, meanwhile the balance power P_b is regulated to track its reference P_b^* very well, which also validates the maximum balance power is the

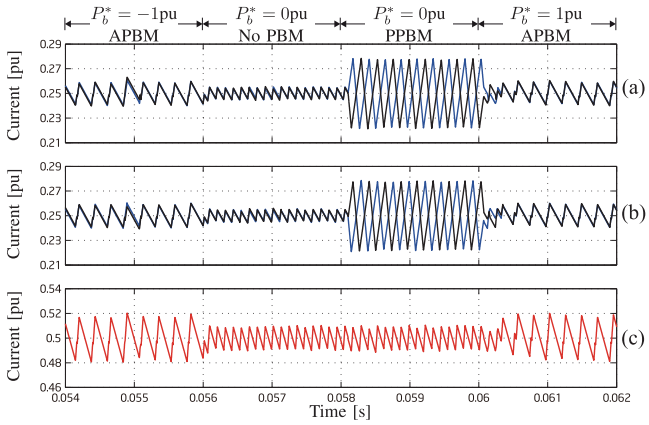

Fig. 16. Simulated dynamic performance of the output currents in CV mode, for $d > 0.5$. (a) Unit 1 output currents i_{op1} and i_{on1}. (b) Unit 2 output currents i_{op2} and i_{on2}. (c) Total output current i_o.

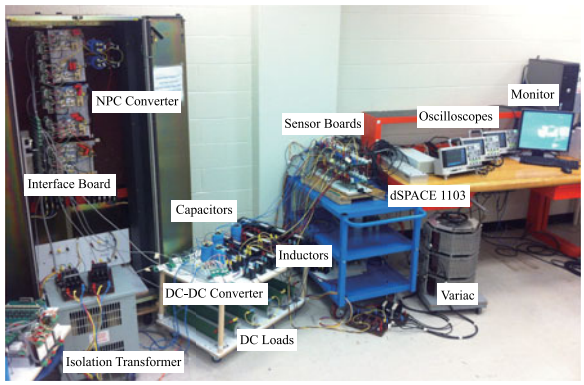

Fig. 17. Photograph of the experimental setup.

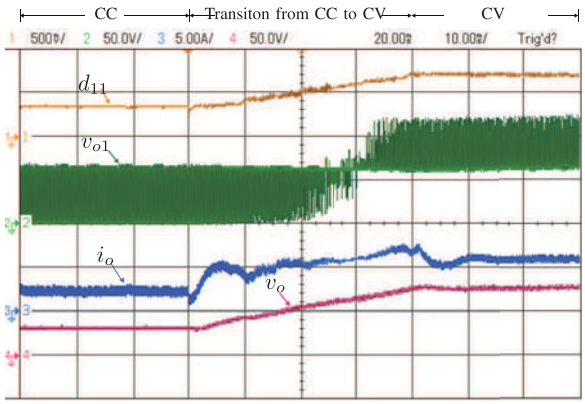

Fig. 18. Experimental results for the transition from CC mode to CV mode. Ch1: modulation signals d_{11} (0.5/div), Ch2: unit 1 output voltage v_{o1} (50 V/div), Ch3: total output current i_o (5 A/div), Ch4: output voltage v_o (50 V/div). Time scale: 10 ms/div.

output power when $d < 0.5$. Moreover, it becomes clear that, under PPBM, the total neutral-point current i_{np} is zero, hence decreasing the power and voltage fluctuations at the dc-side, compared with its value when no PBM is used under balanced power conditions.

The evolution of the internal control signals is presented in Fig. 12. It can be seen that Δd_1 varies from its minimal value to its maximum in order to generate the maximum balance power as presented in Fig. 11(b). As the APBM is activated, the power balance control signal Δd_1 is regulated in order to have a positive average value in the total neutral-point current from 0.028 to 0.030 s and a negative average value from 0.034 to 0.036 s as showed early. Then, when no PBM is performed actively, Δd_1 is zero so d_{11} and d_{14} are equal to $\bar{d}_{11}$ and $\bar{d}_{14}$, respectively, as shown in Fig. 12(c).

Finally, the output currents are presented in Fig. 13. It can be seen that the current sharing between the two units is successfully achieved. Compared with no PBM, the APBM makes each unit output currents ripple larger, leading also to the larger total output current ripple. On the other hand, it is also evident how PPBM results in higher ripple on each unit output current but the total output one is unaltered, which is consistent with the analysis in Section IV-B. Finally, it can be seen from Figs. 11 to 13 that the transition between APBM and PPBM is rather smooth.

Figs. 14 to 16 present the performance of the converter when operating in the CV mode, and $d > 0.5$. Fig. 14(a) shows that the output voltage is controlled to track its reference $v_o^* = 2$ p.u., and despite $P_b^* = \pm 1$ p.u., P_b only reaches its maximum achievable value of $0.\bar{6}$p.u., as established in (4). The same dc power balance management transitions take place as in the previous scenario as presented in Fig. 14(b). It should be mentioned that for a practical charging station with all fast chargers based on the proposed dc–dc converter, such an unbalanced scenario rarely happens in the proposed charging station architecture. This is because the fast chargers (which are the critical loads on the system) do not contribute to the unbalance problem and also themselves can do most of the balance task, any additional balancing capability is covered by the NPC converter, so no additional balancing circuit is needed for practical development.

Fig. 15 presents the evolution of the controlled variables, and in this case Δd_1 fluctuates from -0.4 to 0.4, when P_b^* is -1 and 1 p.u., respectively, in order to perform the power balance tasks, as shown in Fig. 14(b). The controller modifies d_{11} and d_{14} in such a way that i_{np} has a positive average value between 0.054 and 0.056 s, and a negative one in the period between 0.060 and 0.062 s. Just as the previous scenario, the average values of modulation signals d_{11} and d_{14} have no difference when deactivating the power balance management, as it can be seen in Fig. 15(b) and (c).

Similar to the CC mode, in the CV mode, the current balance between the two units is also reached well, as shown in Fig. 16. Moreover, PPBM can also eliminate the fluctuant neutral-point currents and keep total current ripple unchanged at the expense of a little increase in the current ripple of each unit; while APBM leads to increased ripples both on the unit output current and on the total output current. The presented results verify the principle and performance of the proposed converter with comprehensive dc power balance management, which are consistent with the theoretical analysis in the previous sections.

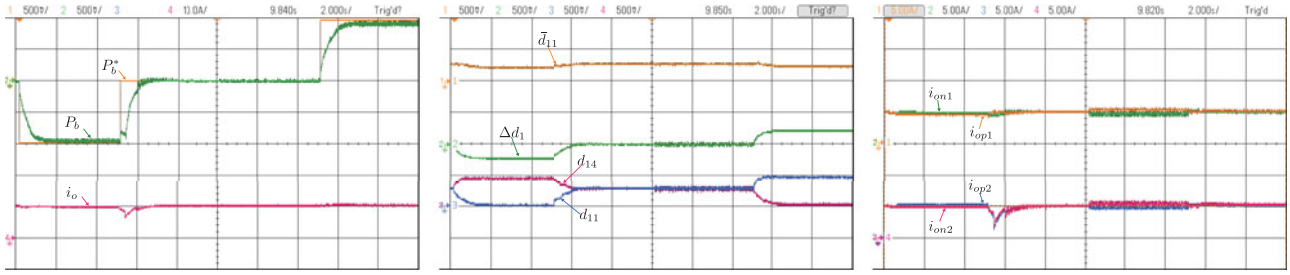

Fig. 19. Experimental dynamic performance of dc power balance managements in CC mode, for $d \leq 0.5$. (a) Ch1: balance power reference P_b^* (0.5/div), Ch2: balance power P_b (0.5/div), Ch4: total output current i_o (10 A/div). (b) Ch1: original modulation signal $\bar{d}_{11}$ (0.5/div), Ch2: power balance control signal Δd_1 (0.5/div), Ch3: final modulation signal d_{11} (0.5/div) and Ch4: final modulation signal d_{14} (0.5/div). (c) Ch1: unit 1 output current i_{op1} (5 A/div), Ch2: unit 1 output current $i_{\mathrm{on}1}$ (5 A/div), Ch3: unit 2 output current i_{op2} (5 A/div), CH4: unit 2 output current $i_{\mathrm{on}2}$ (5 A/div). Time scale: 2 s/div.

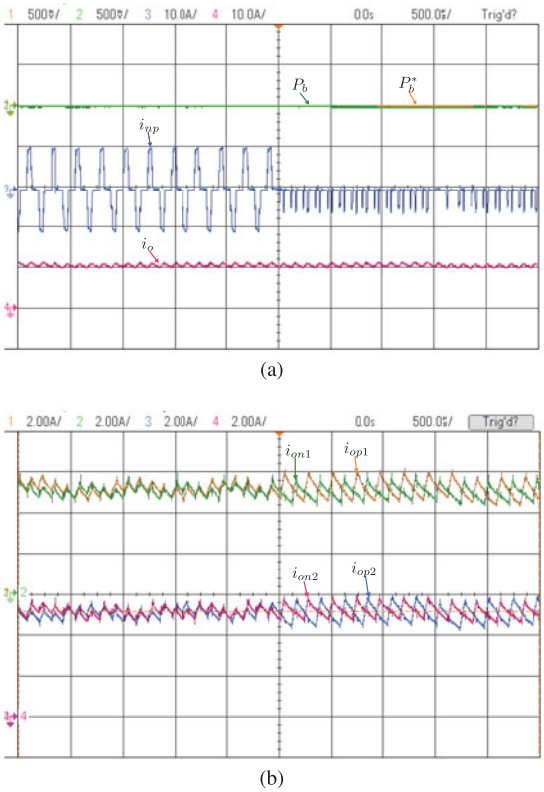

Fig. 20. Experimental results of APBM to PPBM in CC mode for $P_b^* = 0$. (a) Ch1: balance power reference P_b^* (0.5/div), Ch2: balance power P_b (0.5/div), Ch3: total neutral-point current i_{np} (10 A/div), Ch4: total output current i_o (10 A/div). (b) Ch1: unit 1 output current i_{op1} (5 A/div), Ch2: unit 1 output current $i_{\mathrm{on}1}$ (5 A/div), Ch3: unit 2 output current i_{op2} (5 A/div), CH4: unit 2 output current $i_{\mathrm{on}2}$ (5 A/div). Time scale: 500 μs/div.

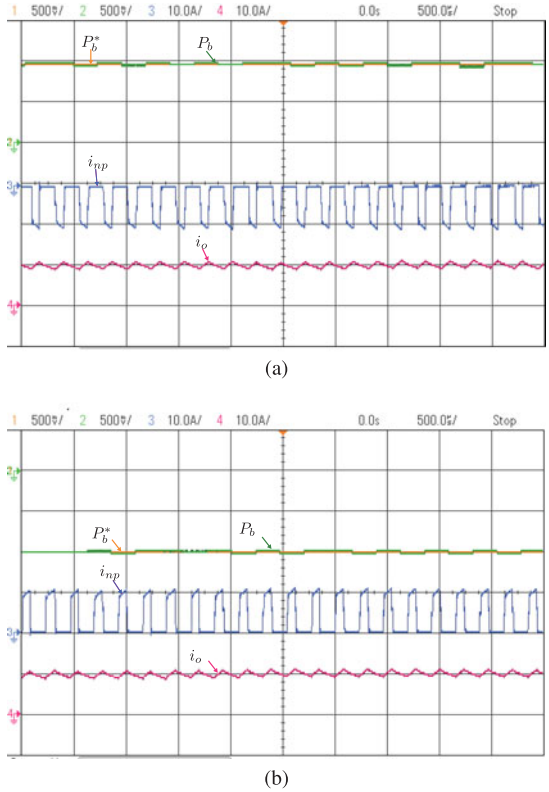

Fig. 21. Experimental results of APBM in CC mode. (a) For $P_b^* = 1$, Ch1: balance power reference P_b^* (0.5/div), Ch2: balance power P_b (0.5/div), Ch3: total neutral-point current i_{np} (10 A/div), Ch4: total output current i_o (10 A/div). (b) For $P_b^* = -1$, Ch1: balance power reference P_b^* (0.5/div), Ch2: balance power P_b (0.5/div), Ch3: total neutral-point current i_{np} (10 A/div), Ch4: total output current i_o (10 A/div). Time scale: 500 μs/div.

VII. Experimental Results

The final step for validating the proposed three-level dc–dc converter based fast charger with comprehensive dc power balance management is through experimental testing. In order to perform the experiments, a 1.2-kW setup has been implemented as shown in Fig. 17. The key parameters of the converter are given in Table I, which were designed accordingly in order to have an accurate representation of the final application. Fig. 17 shows that the setup is composed of an isolation transformer, inductive filters, an IGBT based NPC converter to provide a bipolar dc bus, a parallel three-level dc–dc converter which is feeding resistive loads. The control platform is based on a dSPACE which samples the voltages and currents through a sensor board, performs the control algorithms and the modulation, then sends gating signals for IGBTs through an interface board.

Similar to the simulation, the converter starts operating in CC mode, then ends operating in CV mode, and in each mode, the four scenarios stated in the simulation section are forced to

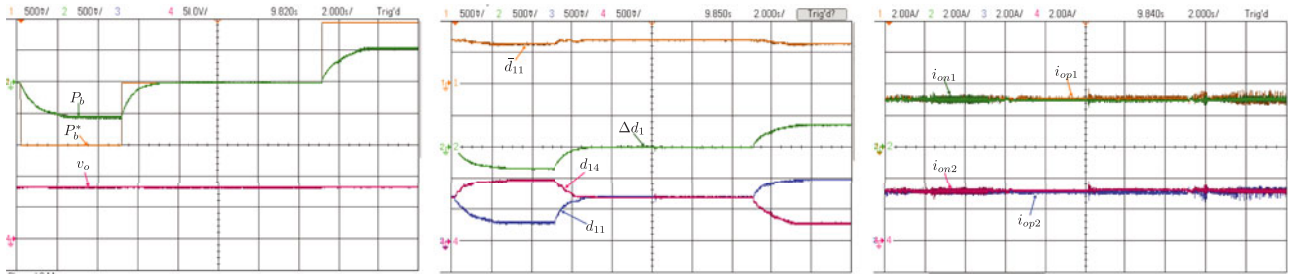

Fig. 22. Experimental dynamic performance of dc power balance managements in CV mode, for $d > 0.5$. (a) Ch1: balance power reference P_b^* (0.5/div), Ch2: balance power P_b (0.5/div), Ch4: output voltage v_o (50 V/div). (b) Ch1: original modulation signal $\bar{d}_{11}$ (0.5/div), Ch2: power balance control signal Δd_1 (0.5/div), Ch3: final modulation signal d_{11} (0.5/div), Ch4: final modulation signal d_{14} (0.5/div). (c) Ch1: unit 1 output current i_{op1} (2 A/div), Ch2: unit 1 output current $i_{\mathrm{on}1}$ (2 A/div), Ch3: unit 2 output current i_{op2} (2 A/div), CH4: unit 2 output current $i_{\mathrm{on}2}$ (2 A/div). Time scale: 2 s/div.

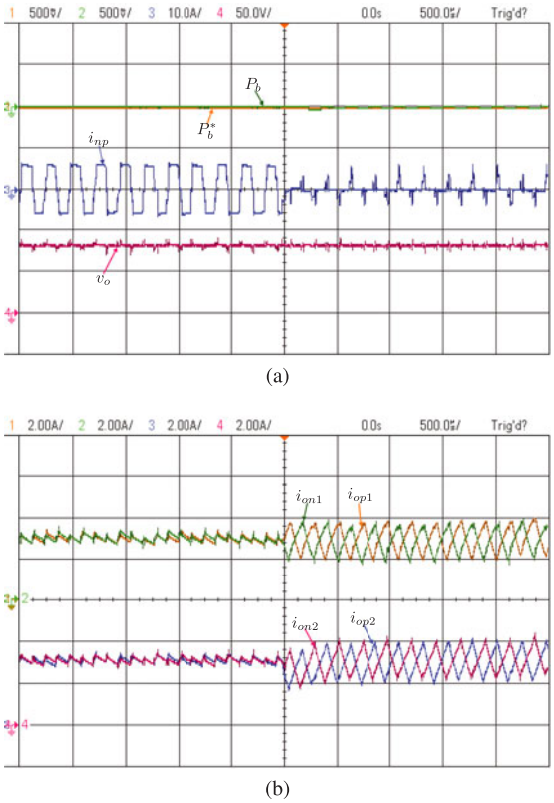

Fig. 23. Experimental results of APBM to PPBM in CV mode for $P_b^* = 0$. (a) Ch1: balance power reference P_b^* (0.5/div), Ch2: balance power P_b (0.5/div), Ch3: total neutral-point current i_{np} (10 A/div), Ch4: output voltage v_o (50 V/div). (b) Ch1: unit 1 output current i_{op1} (2 A/div), Ch2: unit 1 output current $i_{\mathrm{on}1}$ (2 A/div), Ch3: unit 2 output current i_{op2} (2 A/div), CH4: unit 2 output current $i_{\mathrm{on}2}$ (2 A/div). Time scale: 500 μs/div.

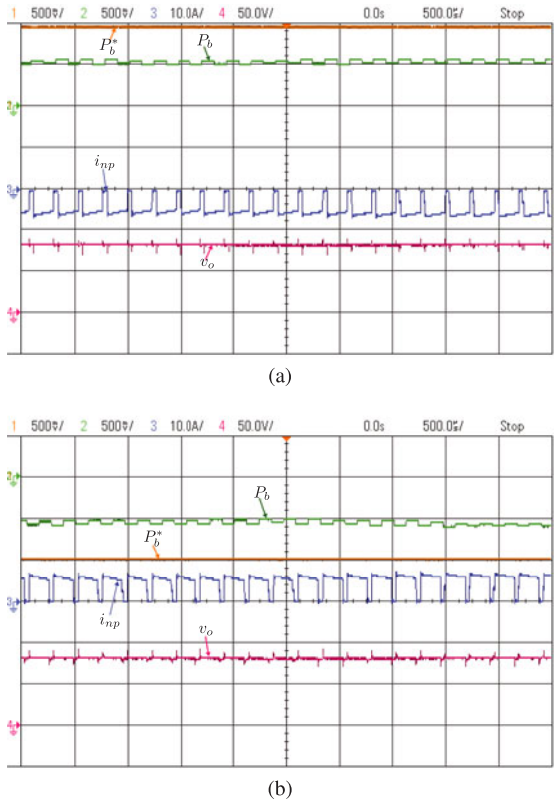

Fig. 24. Experimental results of APBM in CV mode. (a) For $P_b^* = 1$, Ch1: balance power reference P_b^* (0.5/div), Ch2: balance power P_b (0.5/div), Ch3: total neutral-point current i_{np} (10 A/div), Ch4: output voltage v_o (50 V/div). (b) For $P_b^* = -1$, Ch1: balance power reference P_b^* (0.5/div), Ch2: balance power P_b (0.5/div), Ch3: total neutral-point current i_{np} (10 A/div), Ch4: output voltage v_o (50 V/div). Time scale: 500 μs/div.

verify the proposed dc power balance management. Figs. 18 to 24 reveal that the overall behavior of the experimental results is very close to the simulated ones.

Fig. 18 presents the transition operation from CC mode to CV mode, and the changes in the duty cycle show that the transition between these modes is rather smooth and controlled during all the time. As expected, it can be seen how v_{o1} presents three voltage levels on its waveform, similar with the simulation ones.

At the beginning of the test, the system is operating in CC mode, and by analyzing the balance power P_b plotted in Fig. 19(a), it can be seen how it perfectly tracks its reference P_b^* (both P_b and P_b^* are normalized to the actual output power P_o), during which the total output current i_o is controlled tightly to be its reference i_o^*=10 A. Please note that, as during this mode $d \leq 0.5$, the maximum balance power matches the output power. The inner modulation signals are presented in Fig. 19(b), where Δd_1 varies accordingly depending on the operation mode, being consistent with the simulated case. In addition, the evolution of the output currents i_{op1}, $i_{\mathrm{on}1}$, i_{op2} and $i_{\mathrm{on}2}$ in Fig. 19(c) allows confirming the proper current sharing between the two units.

The transition from APBM to PPBM is shown in Fig. 20. As stated earlier, the total neutral-point current i_{np} exhibits a big pulsating waveform when $P_b = 0$ and APBM is activated under balanced power conditions, while during PPBM i_{np} is virtually zero as presented in Fig. 20(a). It is also worth noting how the total output current ripple keeps unchanged, although each unit output current ripple becomes a little larger during PPBM as shown in Fig. 20(b), which coincides with the aforementioned theoretical analysis and simulation waveforms.

The operation of APBM in CC mode is presented in Fig. 21 and the power balance reference P_b^* is set to ± 1, respectively. It becomes clear how the converter is demanding power from the positive dc bus, as i_{np} exhibits a negative average value when $P_b^* = 1$ as shown in Fig. 21(a). The opposed scenario $P_b^* = -1$ is appreciated in Fig. 21(b), as the pulsating current i_{np} shows a positive mean value, hence the converter demands energy from the negative dc bus.

Then, the dc power balance managements in CV mode is verified through Figs. 22 to 24. Just as in the previous case, the evolution of P_b is presented in Fig. 22(a), and despite its command $P_b^* = \pm 1$ it only sets in its maximum achievable value, as defined in (4). During the whole process, the output voltage is accurately controlled to 80 V. The dynamic performance of the inner modulation signals Δd_1, d_{11} and d_{14} from Fig. 22(b) presents a consistent behavior with the simulation results. Meanwhile, the current sharing is also confirmed in Fig. 22(c).

Fig. 23 provides the experimental results of the transition from APBM to PPBM in CV mode, showing how the fluctuating pulses in i_{np} have been eliminated, while the output currents of each unit exhibit similar behaviors to the simulation ones.

Finally, the experimental waveforms of operation under APBM when $P_b^* = \pm 1$ are shown in Fig. 24. It can be seen that all the pulses of i_{np} are negative when $P_b^* = 1$ as shown in Fig. 24(a), while positive when $P_b^* = -1$ as shown in Fig. 24(b), which means the converter provides the maximum balance power as it can.

VIII. Conclusion

The high-power three-level dc–dc converter based fast charger with comprehensive dc power balance management is proposed for high-power charging stations with a bipolar dc bus. The proposed fast charger has the dc power balance capability and enables the elimination of additional balancing circuits and high-frequency transformers, thereby improves the overall system efficiency. It gives the central NPC converter more freedom to control grid-side currents, so enhances the power quality. Meanwhile, the use of parallel three-level dc–dc converters brings lower current stress and lower output current ripples, and the power capacity can be easily scaled up due to its modularity.

Both the active and passive dc power balance managements (APBM and PPBM) are proposed. Their operating principles and the efficient cooperation between them are studied. The idea of PBMC is introduced for the charging station, and the overall control diagram for fast chargers is developed. The APBM is proposed to assist the central NPC converter in balancing power when the imbalanced power is out of its predetermined controllable zone; while the PPBM is proposed to ensure the balanced operation of fast chargers themselves and eliminate the drastic fluctuant neutral-point currents so as to decrease the dc-side capacitors requirement. The power balance limits of APBM are explored for the PBMC to allocate the power balance tasks among the operating fast chargers and the central NPC converter. Meanwhile, the circulating currents of PPBM are also analyzed. Through the simulation and experimental results, it has been demonstrated that the proposed fast charger performs very well in achieving the comprehensive dc power balance management in addition to the basic function of EV fast charging.

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Longcheng Tan (S'08–M'13) was born in Henan, China, in 1983. He received the B.Eng. degree in electrical engineering from the Beijing Institute of Petrochemical Technology, Beijing, China, in 2004, and received the Ph.D. degree in power electronics and power drives from the Institute of Electrical Engineering, Chinese Academy of Sciences (IEECAS), Beijing, China, in 2009.

He worked at the Power Electronics and Electrical Drives Research Center, IEECAS, from 2009 to 2014, where he became an Associate Professor in 2012. He is currently a Postdoctoral Fellow at the Laboratory for Electric Drive Applications and Research and Center for Urban Energy, Ryerson University, Toronto, ON, Canada. His research interests include high power converters, power quality, motor drives, and electric vehicles.

Bin Wu (S'89–M'92–SM'99–F'08) received the M.A.Sc. and Ph.D. degrees in electrical and computer engineering from the University of Toronto, Toronto, ON, Canada, in 1989 and 1993, respectively.

In 1993, he joined Ryerson University, Toronto, where he is currently a Professor and Senior NSERC/Rockwell Automation Industrial Research Chair in power electronics and electric drives. He has published more than 300 technical papers, authored/coauthored two Wiley-IEEE Press books, and holds more than 25 issued/pending patents in the area of power conversion, medium-voltage drives, and renewable energy systems.

Dr. Wu received the Gold Medal of the Governor General of Canada in 1993, Premier's Research Excellence Award in 2001, NSERC Synergy Award for Innovation in 2002, Ryerson Distinguished Scholar Award in 2003, YSGS Outstanding Contribution to Graduate Education Award, and the Professional Engineers Ontario Engineering Excellence Medal in 2014. He is a Fellow of the Engineering Institute of Canada and the Canadian Academy of Engineering.

Sebastian Rivera (S'10) was born in Valparaiso, Chile, in 1986. He received the B.Sc. and M.Sc. degrees in electronics engineering from Universidad Tecnica Federico Santa Maria, Valparaiso, in 2007 and 2011, respectively. He is currently working toward the Ph.D. degree in electrical and computer engineering at the Centre for Urban Energy, Ryerson University, Toronto, ON, Canada.

His research interests include multilevel converters, renewable energy conversion systems and electric vehicles.

Mr. Rivera received the Emerging Leaders in the Americas Program Scholarship from the Canadian Bureau for International Education in 2010, the Ph.D. Scholarship from the Chilean National Commission for Scientific and Technological Research in 2011, and the 2013 Graduate Research Excellence Award from Ryerson University.

Venkata Yaramasu (S'08–M'14) was born in Guntur, India. He received the B.Tech. degree in electrical and electronics engineering from Jawaharlal Nehru Technological University, Hyderabad, India, in 2005, the M.E. degree in electrical engineering with specialization in power electronics from the S. G. S. Institute of Technology and Science, Indore, India, in 2008, and the Ph.D. degree in electrical engineering from Ryerson University, Toronto, ON, Canada, in 2014.

He is currently a Postdoctoral Research Fellow at the Laboratory for Electric Drive Applications and Research and the Center for Urban Energy, Ryerson University. His research interests include renewable energy, high power converters, electric vehicles, and predictive control.

Dr. Yaramasu received six Best Student Paper Awards, and two first prizes in national level technical quiz competitions during his undergraduate studies in India. During his Ph.D. studies at Ryerson University, he received the Best Poster Award at the Natural Sciences and Engineering Research Council of Canada—Wind Energy Strategic Network Annual Meeting 2010, Best Poster Awards from the Electrical and Computer Engineering Department and Faculty of Engineering and Architectural Science in 2013, Student Research Awards from the Toronto Hydro, Hydro One and Connect Canada in 2010, 2012 and 2013, Research Excellence Awards from the ECE Department in 2012, 2013 and 2014, and Best Teaching Assistant Award from the FEAS in 2010.