Electric Vehicle Charging Station Using a Neutral Point Clamped Converter With Bipolar DC Bus

Sebastian Rivera, *Student Member, IEEE*, Bin Wu, *Fellow, IEEE*, Samir Kouro, *Member, IEEE*, Venkata Yaramasu, *Member, IEEE*, and Jiacheng Wang, *Member, IEEE*

***Abstract*—This paper proposes a novel architecture for plug-in electric vehicles (PEVs) dc charging station at the megawatt level, through the use of a grid-tied neutral point clamped (NPC) converter. The proposed bipolar dc structure reduces the step-down effort on the dc–dc fast chargers. In addition, this paper proposes a balancing mechanism that allows handling any difference on the dc loads while keeping the midpoint voltage accurately regulated. By formally defining the unbalance operation limit, the proposed control scheme is able to provide complementary balancing capabilities by the use of an additional NPC leg acting as a bidirectional dc–dc stage, simulating the minimal load condition and allowing the modulator to keep the control on the dc voltages under any load scenario. The proposed solution enables fast charging for PEVs concentrating several charging units into a central grid-tied converter. In this paper, simulation and experimental results are presented to validate the proposed charging station architecture.**

***Index Terms*—Bipolar dc bus, fast charging, grid connection, neutral point clamped (NPC), plug-in electric vehicles (PEVs).**

I. Introduction

DUE to the key role that transportation represents to modern society, the search for alternatives on its energy sources has become an important topic for both industry and academia over the last decades. The strong dependence on the gasoline supply chain along with the rapid depletion of oil reserves, a growing environmental concern, and the continuous rise in the price of gasoline have led to the development of alternative car technologies (electric, hydrogen, biofuels, etc.). Special attention has been given to the electric vehicle (EV) concept, as the most likely replacement to conventional internal combustion engine vehicles, because of its strong potential to deliver mainstream products for large-scale deployment [1]. This is supported by studies highlighting the benefits of a strong penetration of EVs in the transportation fleet [2], [3] particularly as we move toward cleaner electricity generation [4].

However, despite that the consumers are well aware of these benefits, they are still more inclined to the use of conventional cars. This is mainly due to the limited mileage capacity offered by the batteries and their long charging processes (over 4 h) using conventional Level-I and Level-II chargers [1], [5], [6]. A key factor in a larger PEV penetration thus is the development and availability of fast charging architectures that will enable replenishing the batteries in reduced times, comparable to a stop at a gas station [6]–[8].

Nevertheless, the fast charging process not only represents challenges for the vehicle itself but also involves the electric system. To start with, the power ratings involved make it unlikely to be adopted as an on-board solution, due to the requirement for larger, heavier, and costly additional equipment [6]. Furthermore, it is not suitable to be a residential application since its inherent three-phase structure and also because of the transformers of these areas are not designed to meet this important increase on the power levels [1]. Finally, from the grid point of view, the penetration of PEVs will require additional generation or energy storage units, as the actual electric system will not be able to satisfy the demand, particularly at peak consumption hours. These reasons have led to the concept of a commercial charging station with several off-board high power chargers, similar to conventional gas filling stations located at public places (parking lots, work, shopping locations, rest stops along highway, etc.) as a viable solution to enable PEV fast charging.

The structure of this charging station can either be with an ac bus, where each charging unit is fed by its independent ac–dc stage, or each unit connected to a common dc bus enabled by a single ac–dc stage with higher power ratings. The latter option appears as the viable solution due to the nature of the loads, and also presents advantages in terms of cost, efficiency and size, as fewer conversion stages are needed [8]–[10]. Moreover, this structure facilitates the integration of distributed generation or energy storage systems [8], [9].

The central converter stage plays a fundamental role in the charging architecture and is desirable to provide several

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S. Rivera, B. Wu, and V. Yaramasu are with the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON M5B 2K3, Canada (e-mail: srivera@ee.ryerson.ca; bwu@ee.ryerson.ca; vyaramas@ee.ryerson.ca).

S. Kouro is with the Department of Electronics Engineering, Universidad Tecnica Federico Santa Maria, Valparaiso 110-V, Chile (e-mail: samir.kouro@ieee.org).

J. Wang is with the School of Mechatronic Systems Engineering, Simon Fraser University, Vancouver, BC V3T 0A3, Canada (e-mail: jwa156@sfu.ca).

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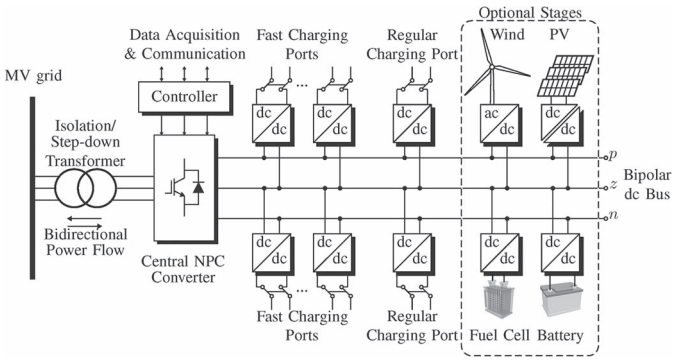

Fig. 1. Proposed charging station with bipolar dc bus.

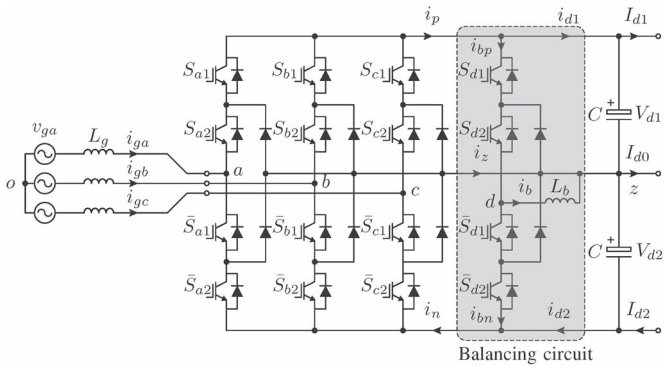

Fig. 2. Grid-tied three-phase NPC converter with a balancing leg.

features as low distortion operation, high power capability, fully adjustable power factor, and to reduce the size of the input filters, while featuring a reduced number in both active and passive components. Among the alternatives, conventional two-level voltage source converter might arise; however, it has a limited capacity to fulfill power ratings, power quality, and efficiency requirements due to semiconductors voltage/currents limits [11]. Other works propose the use of a 12-pulse diode bridge rectifier, improving its harmonic performance through the use of an active filter stage [8]. However, the lack of power factor control and its unidirectional power-flow capability reduces the potential of the charging station.

This work proposes the neutral point clamped (NPC) converter as the rectifier stage, as it shows several advantages: higher grid power quality (three levels), reduced total harmonic distortion (THD), lower switching frequency, medium-voltage (MV) and high-power operation, lower transformer ratio, etc. [12]–[19]. In addition, the power can be scaled up for a larger charging station, hence facilitating the charging of a higher number of PEVs.

This paper proposes a different dc-bus charging station concept, using a bipolar dc bus, enabled by a grid-tied NPC. This increases the power capacity of the station to megawatt level as the dc-link voltage is doubled. However, the step-down effort of the battery chargers is maintained as they are connected to the split dc bus. Despite that the NPC presents a limited capacity of operation under different dc loads, a voltage balancing circuit is implemented to overcome this issue, working only when the system is driven out of the balanced zone. This enables the use of the bipolar structure under any load scenario while keeping the high-quality input currents generated at the ac side and protecting the converter. The proposed architecture is validated using both simulation and experimental results, confirming the capability of working under any load scenario.

II. Bipolar DC Bus Architecture

The proposed charging station architecture is shown in Fig. 1, where a central converter acts as a grid interface, and provides dc power to several charging ports. These charging units can be either conventional or fast chargers, each one with its own independent dc–dc stage. The dc-grid architecture features also the connection of distributed power systems, such as renewable energy generators (PV and wind) and also energy storage devices, as suggested in [20] and [21].

Regarding to the dc structure, the use of a split dc bus offers more flexibility compared with the unipolar dc as it allows the connection of the loads to two regulated voltages: between the neutral point and either the positive or negative bar; or between the positive and the negative bars [22]. Furthermore, this configuration also allows the connection of the station to higher ac voltages, while maintaining the step-down effort of the dc–dc stages. This also has an impact on the power handling capabilities as the connection to higher ac voltages allows higher power without excessive currents and does not need to parallel devices or converters. As the bipolar structure is adopted, the balance control becomes essential [23].

Furthermore, this charging station concept allows several opportunities to provide support to the grid, such as peak power shaving, frequency regulation, reactive compensation, and power fluctuation minimization. In addition, further developments of energy storage devices (batteries and supercaps) will make it possible to provide power back to the grid, enabling vehicle-to-grid (V2G) operation.

A. Central Grid-Tied Converter

To act as the grid interface a four-leg three-phase NPC converter has been selected because it offers superior harmonic performance and higher power handling capabilities [12]–[14]. An additional leg is incorporated to act as a balancing circuit. The scaling of the system is thus made possible, allowing to extend the power level if needed. The converter topology is illustrated in Fig. 2.

According to [13], the correct performance of the NPC is only guaranteed with the accurate control of its midpoint voltage. Because of this, multiple solutions can be found in the literature [15]–[19], which usually solve the problem in the modulation stage with the implementation of a simple balancing mechanism. It is important to note that these schemes are mostly designed considering that the system is being used as a unipolar dc bus, either as a rectifier or in back-to-back configuration. Considering the architecture of the system and also the nature of the application, the fact that the system provides a bipolar dc bus, and each voltage feeds different loads, unbalanced operation is inherent to the system. This is because the origin of the unbalances is the circulation of

currents through the neutral point of the converter, a situation that is imposed by the bipolar configuration. This effect can be mitigated by alternating the connection of the loads to the dc buses. Nevertheless, even if this connection is promoted, unbalance operation will still occur. Therefore, despite that the modulation stage performs the balancing corrections to keep the voltage controlled, the unbalanced scenarios that the system is able to overcome are limited [21]. This limitation will be studied in detail in the following sections.

B. NPC Bipolar Unbalance Limitation

The system and its variable definitions are presented in Fig. 2, where the dc power demanded by the loads is defined as

$$P_d = V_{d1} I_{d1} + V_{d2} I_{d2}. \tag{1}$$

Moreover, the NPC requires a proper balance on its dc voltages for correct operation; thus, it is assumed for the rest of the analysis that this condition is met. This means that $V_{d1} = V_{d2} = V_d/2$, which leads to

$$P_d = \frac{V_d}{2}(I_{d1} + I_{d2}). \tag{2}$$

Due to the nature of the application, the study of the unbalance operation becomes relevant. During balanced operation, the current flowing through the neutral point I_{d0} is approximately zero, and the balancing of the midpoint is similar to the one needed in the unipolar architecture. However, the presence of unbalances results in current flowing through this point, increasing the possibilities of drifts in the dc voltages. To illustrate the balancing capability of the modulation stage, the following case is proposed: Assume that the power demand in the upper dc bus is P_{d1} and kept constant, whereas P_{d2} has been reduced to only a fraction ϵ of it. As the dc voltages remain balanced, the demanded power becomes

$$P_d = \frac{V_d}{2} I_{d1}(1 + \epsilon). \tag{3}$$

On the other hand, the current in the positive bar can be assumed equal to the current demanded by the upper bus; thus, $i_p \approx I_{d1}$ without loss of generality. According to [16], and under unity power factor, i_p is given by

$$i_p = \left(\sqrt{3}m + \frac{6\alpha}{\pi}\right)\frac{I_g}{2}\cos\delta \tag{4}$$

where m stands for the amplitude modulation index, α is the dc drift of the converter voltage during the positive half cycle, I_g is the grid current amplitude, and δ is the phase angle between the converter voltage and the grid voltage vectors. Note that i_p is defined only by the demand on the upper bus; thus, it will not change for variations in the lower one.

The balancing capability of the modulation stage is reflected by (4) as it suggests that, through the injection of a dc bias in the generated voltage, the midpoint can be controlled in a certain range. Nevertheless, this capability is limited by the linear operation of the modulation stage and thus will vary depending on the modulation scheme and the balancing technique; also, it is a function of the amplitude modulation index m.

Going back to the previous case of unbalance, when the demand at the lower bus is ϵP_{d1} and assuming that ϵ is such that the system is at its limit, injecting the largest value of α and keeping the voltages balanced, the current in the positive bar is given by

$$i_p = \left(\sqrt{3}m + \frac{6\hat{\alpha}}{\pi}\right)\frac{I_g}{2}\frac{1+\epsilon}{2}\cos\delta. \tag{5}$$

However, this current must be equal to the one defined by (4) as the demand in the upper bus has not changed. Hence, using (4) and (5) to solve ϵ leads to

$$\hat{\epsilon} = \frac{2\sqrt{3}m}{\sqrt{3}m + \frac{6\hat{\alpha}}{\pi}} - 1 \tag{6}$$

where $\hat{\epsilon}$ is the lowest value for the ratio between P_{d1} and P_{d2} that the modulation stage is able to handle and keep the voltages from drifting. It should be noted that the previous analysis is also valid for the analogous case, when the lighter load is at the upper bus.

The previous analysis states that, if the system is able to operate above the determined value for $\hat{\epsilon}$, the balancing mechanism provided by the modulation stage is enough to keep the voltages controlled. However, it is very unlikely to have a continuous balanced operation; therefore, an additional balancing technique must be included in order to guarantee the proper operation of the converter in any load scenario.

C. Voltage Balancing Circuit

The correct unbalanced operation of the charging station is limited by the modulation stage as shown earlier. However, due to the random arrival of the vehicles to be charged, different battery technologies, etc., there is no way to guarantee that the system will never be driven outside the valid operation zone. Hence, a complementary balancing circuit is needed in order to operate under any load condition.

The idea is to fully use the balancing capabilities of the modulation stage, and if this is not enough to keep the voltages balanced, a virtual impedance will be added in such a way that, when the system leaves the valid operation zone, it demands the minimal current in order to meet the limit. In other words, for the modulation stage, the system keeps operating at the boundary condition.

As in grid connected systems, the modulation index varies slightly because V_d is rarely changed and it only responds to changes in the load demand, which do not reflect important changes on it. Then, it can be assumed constant; hence, the minimal load condition is known *a priori*. In addition, the direction of I_{d0} will change depending on the location of the lighter load (unbalance), making mandatory the bidirectional characteristic of the balancing circuit, to control current in both directions.

To illustrate the proposed balancing mechanism, refer to Fig. 2. As stated earlier, the modulator will provide a certain room to handle different loads through the injection of a dc bias

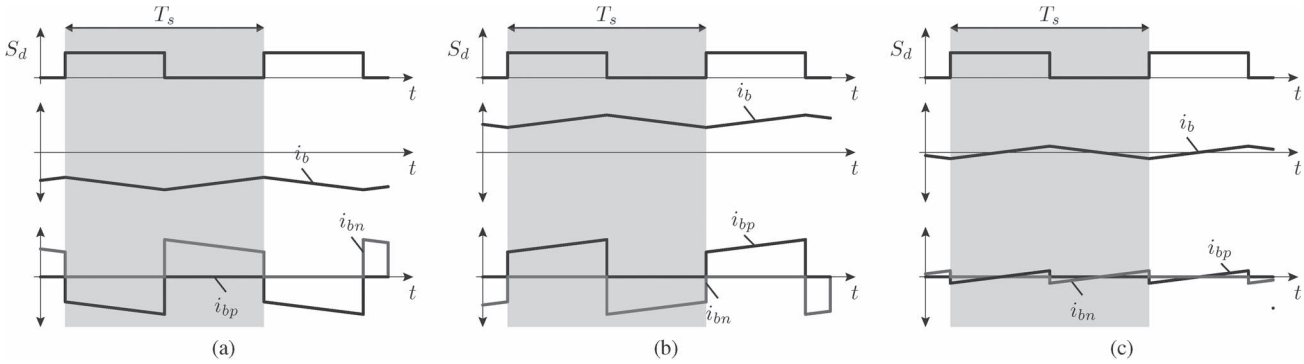

Fig. 3. Different operating conditions of the balancing circuit. (a) Lower bus current compensation. (b) Upper bus current compensation. (c) No current compensation.

in the converter voltage and is limited by the maximum current that can flow through the neutral point. If the unbalance ratio exceeds this operational zone, the voltages will drift no matter the corrections done in the modulation stage. The presence of the balancing leg is then to emulate the minimal load condition. In other words, if the unbalance is present in the lower bus, the maximum current in the neutral point is $I_{d0} = (\hat{\epsilon} - 1)I_{d1}$, and the remanent current $\hat{\epsilon}I_{d1}$ must be conducted through the negative bar in order to maintain the voltages balanced. This principle can be further explained using the signals of Fig. 3. Consider that S_d is the switching function of the upper devices. Given that, in the studied case, the balancing circuit will impose a positive current i_{bn} such as the current in the negative bar is $\hat{\epsilon}I_{d1}$. To do so, the current flowing through the inductor i_b should reverse its polarity, as shown in Fig. 3(a). The analogous scenario shown in Fig. 3(b) is when the unbalance is present in the upper bus, hence imposing a current i_{bp} with positive average value. Finally, Fig. 3(c) presents the operation of the balancing leg during the balanced operation, when no current compensation is needed, making all the currents in the circuit to be zero. Is worth noting how the duty cycle remains fixed at 0.5 in all the scenarios, as the dc–dc stage is connected between the full dc voltage of the converter and its midpoint.

This balancing circuit can be implemented in several ways. In [24], a bidirectional boost converter is employed in a five-level NPC. For simplicity, this proposal uses a fourth leg in the NPC, which is operated as a bidirectional dc–dc converter, as shown in Fig. 2. Using a leg identical to the other phases of the circuit facilitates design and implementation through power electronic building blocks. This is a desirable characteristic in practical applications rather than hybrid converters.

III. Proposed Control Scheme

A. Voltage Oriented Control

For the regulation of the grid-connected converter, the voltage oriented control (VOC) scheme shown in Fig. 4 is used. The modulation stage is based on the space vector modulation (SVM) algorithm in [25], and for the balancing mechanism, through the redistribution of the positive and negative small vectors usage, a proportional–integral (PI) controller has been included.

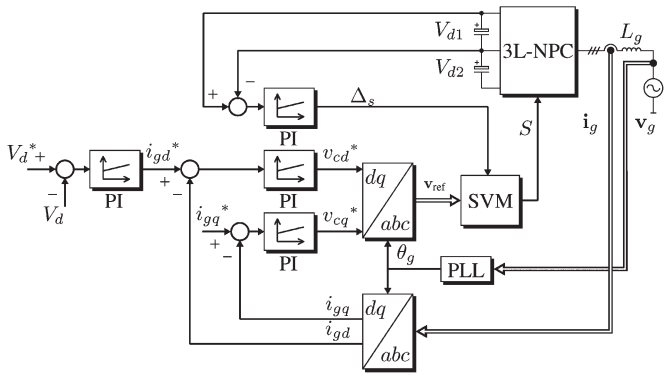

Fig. 4. VOC block diagram for the central NPC converter.

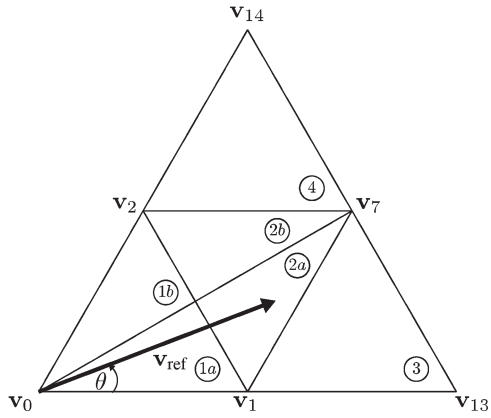

Fig. 5. SVM operating principle in sector I: $\mathbf{v}_{\text{ref}}$ synthesized by $\mathbf{v}_1$, $\mathbf{v}_2$, and $\mathbf{v}_7$.

B. Space Vector Modulation and Load Ratio Limit

As it was mentioned in the previous sections, the modulation stage will provide some balancing capabilities, through the redistribution of the NPC small vectors usage, in order to have a midpoint voltage accurately controlled. This way of balancing does not alter the tracking of the converter voltage reference. To illustrate the principle, consider the situation shown in Fig. 5, where the reference vector can be synthesized as

$$\mathbf{v}_{\text{ref}} = f_{\text{sw}}(t_a\mathbf{v}_1 + t_b\mathbf{v}_2 + t_c\mathbf{v}_7) \tag{7}$$

TABLE I
DWELL-TIME CALCULATION 3L-SVM FOR ODD SECTORS

Reg.	t_a	t_b	t_c
$1a$	$2m\sin(\theta_1-\theta)$	$2m\sin(\theta-\theta_2)$	$1-2m\sin(\theta-\theta_3)$
$1b$	$2m\sin(\theta-\theta_2)$	$1-2m\sin(\theta-\theta_3)$	$2m\sin(\theta_1-\theta)$
$2a$	$1-2m\sin(\theta-\theta_2)$	$1-2m\sin(\theta_1-\theta)$	$2m\sin(\theta-\theta_3)-1$
$2b$	$1-2m\sin(\theta_1-\theta)$	$2m\sin(\theta-\theta_3)-1$	$1-2m\sin(\theta-\theta_2)$
3	$2-2m\sin(\theta-\theta_3)$	$2m\sin(\theta_1-\theta)-1$	$2m\sin(\theta-\theta_2)$
4	$2-2m\sin(\theta-\theta_3)$	$2m\sin(\theta_1-\theta)$	$2m\sin(\theta-\theta_2)-1$

where $\theta_1=\frac{k\pi}{3}$, $\theta_2=\frac{(k-1)\pi}{3}$, $\theta_3=\frac{(k-2)\pi}{3}$ and k stands for the sector number.

Note: The dwell-times are assigned in order, following the seven segment sequence used in [25]. For even sectors the expressions for t_b and t_c have to be swaped.

where f_{sw} is the switching frequency of the SVM algorithm. To determine the maximum injected dc drift, the average usage time for the small vectors t_a is calculated over the positive half cycle. During normal operation and using the example, t_a is equally divided in the redundancies of $\mathbf{v}_1$, $\mathbf{v}_{1\text{N}}$, and $\mathbf{v}_{1\text{P}}$, thus the maximum available time to redistribute is $t_a/2$, and in the extreme cases, it uses exclusively one of the redundancies of $\mathbf{v}_1$. This remaining time is equivalent to the maximum dc drift that can be injected within the linear zone of the modulation and varies with m. In order to obtain this time, the dwell times in Table I for each small vector are averaged during its corresponding interval. The resulting average expression for the maximum voltage drift is defined in

$$\hat{\alpha}=\begin{cases}\frac{-3m+6m\sin\left(\gamma+\frac{\pi}{6}\right)}{\pi}, & m\in\left[0,\frac{1}{2}\right[\\ \frac{\frac{\pi}{2}-3\gamma+3m\left(1-2\cos\gamma+2\sin\left(\gamma+\frac{\pi}{6}\right)+\sqrt{3}\right)}{\pi}, & m\in\left[\frac{1}{2},\frac{1}{\sqrt{3}}\right[\\ \frac{\frac{\pi}{2}+3\gamma-3m\left(1+2\cos\gamma-2\cos\left(\gamma+\frac{\pi}{3}\right)-\sqrt{3}\right)}{\pi}, & m\in\left[\frac{1}{\sqrt{3}},1\right]\end{cases} \tag{8}$$

where γ is the angle at which the change of region occurs and is defined according to

$$\gamma=\begin{cases}\frac{\pi}{6}, & m\in\left[0,\frac{1}{2}\right[\\ \arcsin\left(\frac{1}{2m}\right)-\frac{\pi}{3}, & m\in\left[\frac{1}{2},\frac{1}{\sqrt{3}}\right[\\ \frac{\pi}{3}-\arcsin\left(\frac{1}{2m}\right), & m\in\left[\frac{1}{\sqrt{3}},1\right].\end{cases} \tag{9}$$

As stated earlier, for the regulation for the midpoint voltage, a linear PI controller is being used. This controller modifies the usage of the small vectors as follows:

$$t_{a\text{P}}=\frac{t_a}{2}(1-\Delta_s), t_{a\text{N}}=\frac{t_a}{2}(1+\Delta_s) \tag{10}$$

where Δ_s is the actuation of the PI. Note that these expressions hold for the case when the loads are consuming power from the grid. In the case of having active loads, the sign of Δ_s must be modified accordingly as the effect of the small vectors in the midpoint voltage is reversed.

Taking into account the balancing strategy, and the maximum value of α allowed by the SVM algorithm, it is possible to determine a theoretical value for the critical load ratio $\hat{\epsilon}$ for the NPC, which depends on the modulation index as stated before. This limit operation is illustrated in Fig. 6.

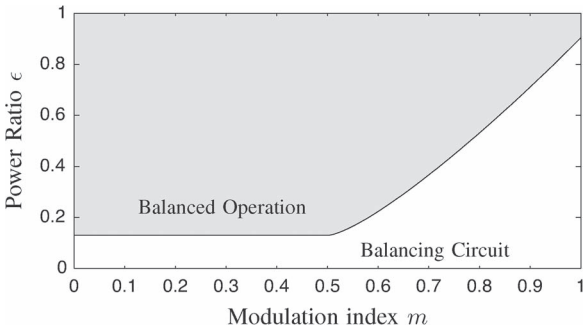

Fig. 6. Critical load ratio for the NPC using SVM.

C. Voltage Balancing Circuit Controller

The idea behind this proposal is to extend the bipolar NPC operation through the entire load range. To do so, the balancing leg must be able to act as a virtual impedance, such that the minimal load condition is met and the modulator is able to keep the voltages balanced. This section explains the generation of the balancing current reference i_b^* in order to ensure the proper operation of the system. This current is related with the equations in (6) and (8). To illustrate the principle, let I_{d1} and I_{d2} denote the currents demanded by the dc loads at upper and lower buses, respectively. In addition, the critical load ratio $\hat{\epsilon}$ is known. First, assume an unbalance is present in the upper bus, such as the modulator is not able to keep the voltages controlled by itself even when injecting the largest value of α. The converter dc currents hold

$$i_p=\hat{\epsilon}i_n. \tag{11}$$

Furthermore, according to Fig. 2, these currents are related with the load currents as follows:

$$i_p=I_{d1}+i_{bp} \tag{12}$$
$$i_n=I_{d2}+i_{bn}. \tag{13}$$

In addition, the operation of the balancing leg is required; therefore, the boost current i_b is different from zero, leading to

$$i_{bn}=-d_b i_b \tag{14}$$
$$i_{bp}=(1-d_b)i_b. \tag{15}$$

However, because of the implementation of the bidirectional dc–dc stage using an additional leg, its duty cycle d_b is fixed to 0.5; hence,

$$i_{bn}=-i_{bp}. \tag{16}$$

Then, by replacing (12) and (13) in (11), and using the information provided by (14)–(16), it is possible to obtain an expression for the required current circulating through the inductor that keeps the system balanced, which is defined as

$$i_b^*=\frac{2\hat{\epsilon}I_{d2}}{(1+\hat{\epsilon})}. \tag{17}$$

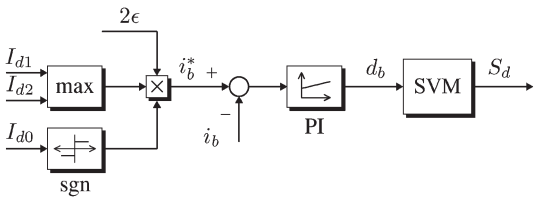

Fig. 7. Voltage-balancing circuit controller for the additional NPC leg.

If the unbalance is at the lower bus, then the balancing circuit should demand a current such that $\hat{\epsilon} i_p$ is flowing through the negative terminal, making i_b negative. This leads to

$$i_b^* = -\frac{2\hat{\epsilon} I_{d1}}{(1+\hat{\epsilon})}. \tag{18}$$

It is important to mention that this current value is the minimal in order to keep the system balanced, making the midpoint PI controller to operate saturated in the unbalanced scenarios. However, as there are other reasons that can drive the system out of balance, such as differences in the capacitance levels of the dc links, a certain room is given to this PI by increasing the demanded current by the boost, in order to guarantee the proper operation of the station in any scenario. Therefore, the boost current reference will be defined as follows:

$$i_b^* = 2\hat{\epsilon} \max\{I_{d1}, I_{d2}\} \text{sgn}(I_{d2} - I_{d1}). \tag{19}$$

A PI controller is used to regulate the input current of the voltage balancing circuit, as presented in Fig. 7. It should be noted that this control scheme only operates when the system is driven outside the gray area of balanced operation shown in Fig. 6. Therefore, an enabling signal is defined as follows:

$$e_B = \begin{cases} 1 & \text{if } |I_{d1} - I_{d2}| > (1-\hat{\epsilon}) \max\{I_{d1}, I_{d2}\} \\ 0 & \text{if } |I_{d1} - I_{d2}| \leq (1-\hat{\epsilon}) \max\{I_{d1}, I_{d2}\}. \end{cases} \tag{20}$$

IV. Simulation Results

The proposed architecture is simulated using MATLAB/Simulink software. A 1.2-MW charging station has been designed for the validation of the proposed architecture, and it is connected to the 4.16-kV grid through a step-down transformer. The SVM algorithm is implemented in order to have an equivalent device switching frequency of 1080 Hz. The parameters of the system are described in Table II.

A. Dynamic Response

The first stage of the validation is the study of the dynamic performance under several load impacts, presented in Fig. 8, a situation that is possible during the sudden connections and disconnections of the EVs for charge because of their random arrival to the station. The following test is performed: The system is assumed in steady state with rated loads on both dc buses (balanced load); then at $t = 0.05$ s, a sudden disconnection of the loads connected to the lower bus takes place, whereas the load is kept at its rated value in the upper dc bus. Next, at $t = 0.1\bar{3}$ s, the unbalance is reversed; now, the rated load is

TABLE II
Simulation and Experimental Parameters

Parameter	Symbol	Value
Grid Voltage Amplitude	V_g	1 pu
Grid Frequency	f_g	1 pu
Input Filter Inductance	L_g	0.1 pu
Input Filter Resistance	R_g	0.02 pu
dc Link Capacitance	C	4.5 pu
dc Link Voltage	V_d	2.174 pu
Boost inductance	L_b	0.36 pu
Switching Frequency	f_{sw}	36 pu
Amplitude Modulation Index	m	0.6408
Frequency Modulation Index	m_f	36
Critical Load Ratio	$\hat{\epsilon}$	0.2829
Simulation Base Voltage	V_B	4160/960 V
Simulation Base Power	P_B	1.2 MW
Experimental Base Voltage	V_B	208 V
Experimental Base Power	P_B	3.6 kW
Base Frequency	f_B	60 Hz

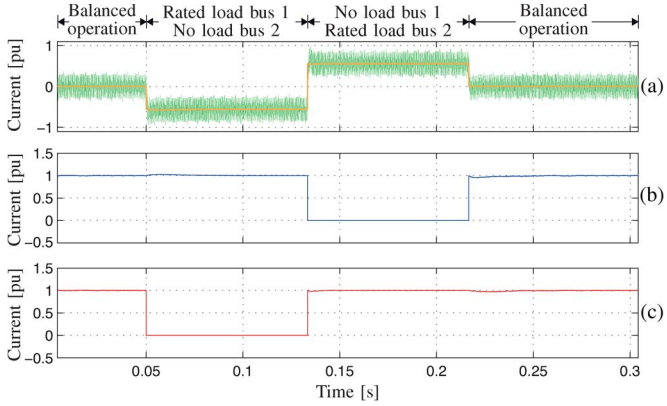

Fig. 8. Simulation results for PEV charging station, dc currents: (a) Boost current i_b and its reference i_b^*. (b) Bus 1 current I_{d1}. (c) Bus 2 current I_{d2}.

connected to bus 2, and no load is connected to bus 1. Finally, at $t = 0.21\bar{6}$ s, both buses return to rated load condition. In addition, to make the scenario more realistic, the grid voltage has been distorted by adding fifth- and seventh-order harmonics, in order to emulate the voltage in the laboratory and keep the comparison fair.

It can be seen that, before $t = 0.05$ s, the currents I_{d1} and I_{d2} are equal; therefore, there is no need to generate a balancing action in the fourth leg. Therefore, boost current i_b is set to zero value. When the first load impact takes place, the current demanded in bus 2 goes to zero as there is no load connected, and as the modulation stage is not able to keep the balance under such condition, the dc–dc stage is commanded to generate a current equal to $-2\hat{\epsilon} I_{d1}$, while I_{d1} is kept constant at rated condition.

Later on, after the second impact at $t = 0.1\bar{3}$ s, the direction of i_b is reversed to compensate the unbalance condition. As the rated load is connected back to lower bus, the reference current becomes $2\hat{\epsilon} I_{d2}$.

Finally, the system is driven back to balance after $t = 0.21\bar{6}$ s, and as there is no need for additional balancing

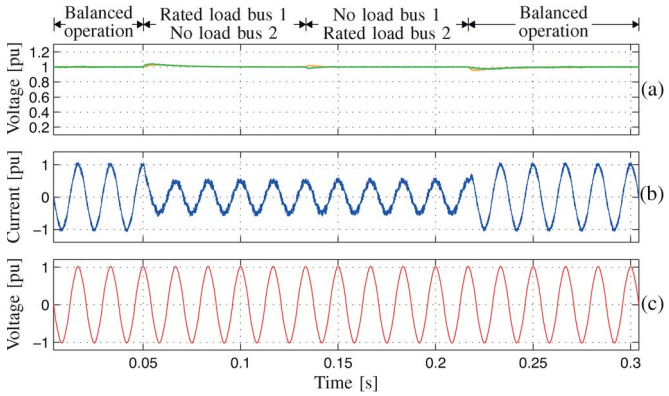

Fig. 9. Simulation results for PEV charging station, VOC signals: (a) DC bus voltages V_{d1} and V_{d2}. (b) Input current i_{ga}. (c) Grid voltage v_{ga}.

capabilities, the control scheme sets the boost current to be zero. Please note that the required current to be drawn by the dc–dc converter is just a fraction of the rated value; thus, the core losses and current stress on the dc choke are lower.

The proper regulation of the boost current i_b leads to balanced capacitor voltages during the whole experiment, as shown in Fig. 9. The dc voltages are maintained at their references, and it is confirmed that the presence of the balancing leg allows to overcome the limitation of the conventional NPC, which is not capable of handling the no load condition in one of the buses while the other is still loaded.

The proper balance of the voltages leads to sinusoidal currents at the input side during the whole operating range, as shown in Fig. 9(b), which shows the waveform of i_{ga}. In addition, it can be seen that, during the mentioned scenarios, the system remains operating with unity power factor, as the current is kept in phase with v_{ga} shown in Fig. 9(c).

B. Steady-State Analysis

In this section, steady-state waveforms of the converter voltage are presented in Fig. 10 to illustrate the balancing mechanism. As the differences between the upper and lower unbalances have already been covered in [21], only one case will be described in detail.

The system behavior for balanced operation is presented in Fig. 10(a). It can be seen that there is no dc drift injected in either of the voltage signals, leading to a symmetrical switching pattern during the positive and negative half-cycles. This is confirmed by the lack of even order harmonics in the spectral components of v_{az}. However, in the presence of load unbalances, the symmetry in the switching pattern is lost because of the redistribution of the small vectors. This situation can be seen in Fig. 10(b)ii, where the no load situation in the lower bus leads to the imposition of a positive dc drift to maintain the voltages balanced. The dc drift becomes obvious by analyzing the voltage spectrum presented in Fig. 10(b)iii. In addition, it is confirmed the balancing method misses the half-wave symmetry, as even-order harmonics appear under the presence of unbalances.

In order to highlight the lack of symmetry during the unbalanced scenario, a detailed waveform is presented in Fig. 11,

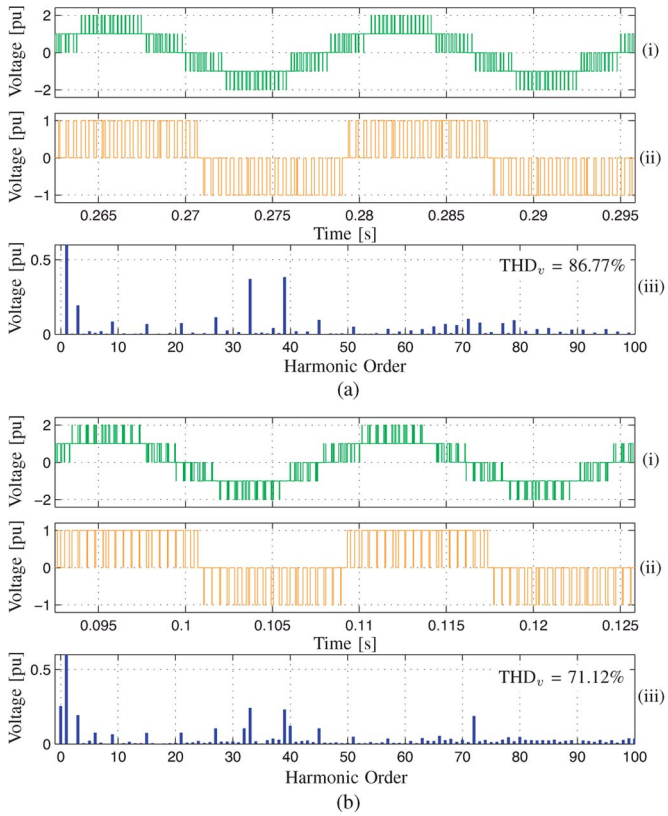

Fig. 10. Steady-state analysis of the converter voltages. i) Line-to-line voltage v_{ab}. ii) Phase voltage v_{az}. iii) Fast Fourier transform (FFT) for v_{az}: (a) Case I, balanced operation; (b) Case II, unbalanced operation in bus 2.

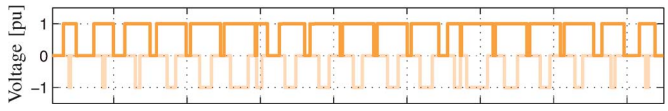

Fig. 11. Converter voltage v_{az} superimposed positive and negative half-cycles during unbalanced operation.

and it can be seen clearly how the pulses in v_{az} become wider during the positive half cycle.

Despite the injection of a dc bias to v_{az} to prevent the drift of the bus voltages, it is confirmed that this effect is not reflected to the line-to-line voltages nor the input currents. This lies in the fact that the method modifies the three phases of the converter identically; therefore, the nonzero dc value is canceled in the phase-to-phase voltages. The waveform for v_{ab} is presented in Fig. 10 for the above two analyzed scenarios, confirming that the balancing action does not introduce a nonzero dc value in the line-to-line voltages.

Finally, the input signals are shown in Fig. 12. Once again, the unity power factor operation of the station is confirmed during the whole test. The waveform for i_{ga} is kept sinusoidal in the three analyzed scenarios, with the corresponding increase in the ripple during the unbalanced operation. Moreover, it can be seen that, under unbalance operation, these currents also show a lack of half-wave symmetry. Detail which is confirmed by its harmonic content presented in Fig. 12(b)iii, which contains even-order harmonics. Nevertheless, cancelation of the triplen harmonics remains under the presence of unbalanced

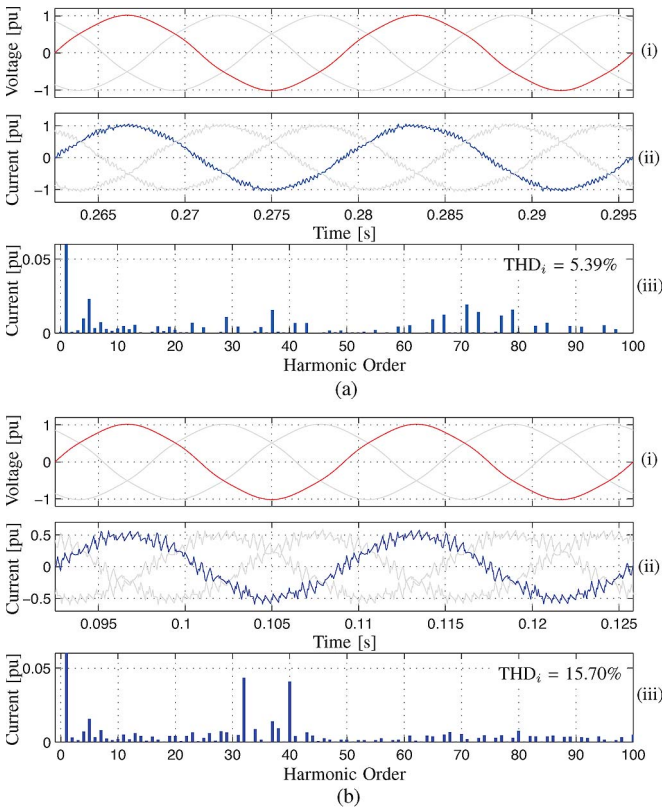

Fig. 12. Steady-state analysis of the input signals. i) Grid voltage v_{ga}. ii) Input current i_{ga}. iii) FFT for i_{ga}: (a) Case I, balanced operation; (b) Case II, unbalanced operation in bus 2.

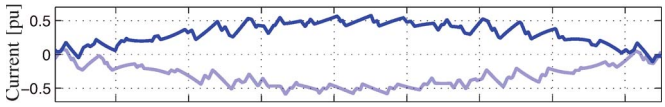

Fig. 13. Input current i_{ga} superimposed positive and negative half-cycles during unbalanced operation.

loads. Fig. 13 emphasizes the nonsymmetrical waveform of i_{ga}, showing the superimposed positive and negative half-cycles and confirming the previous statements.

V. Experimental Results

In order to complete the validation for the proposed architecture, experimental results are obtained using a 3.6-kW four-leg three-phase NPC-based charging station prototype, shown in Fig. 14. As can be seen, the setup consists of an isolation transformer, an inductive filter, an insulated-gate bipolar transistor (IGBT)-based four-leg NPC converter, and a resistive load connected to each dc bus using a relay unit. The control platform used is a dSPACE, which generates the gating pattern for the IGBTs. It is important to mention that the SVM algorithm is programmed to have an equivalent switching frequency of 1080 Hz per device. Using the parameters presented in Table II, the control scheme is applied to the converter. In order to confirm the performance of the voltage balancing under any scenario, a dynamic test is performed similar to the simulation study given in Fig. 8.

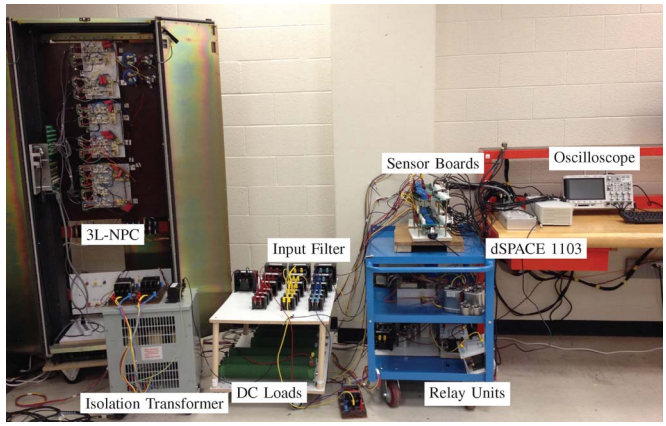

Fig. 14. Experimental setup.

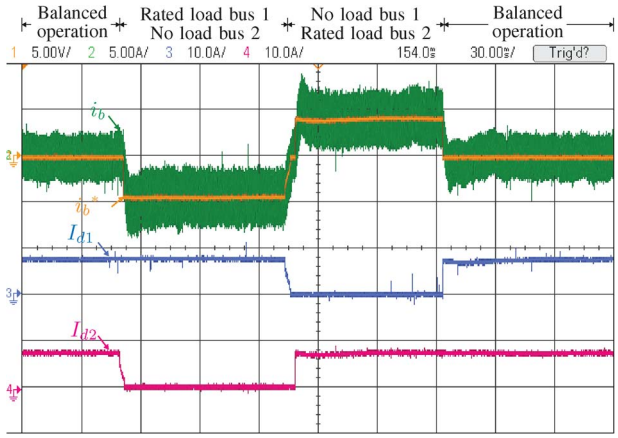

Fig. 15. Experimental results for PEV charging station prototype, dc currents. Ch1 boost current reference i_b^* (5 V/div). Ch2 boost current i_b (5 A/div). Ch3 dc bus 1 load current I_{d1} (10 A/div). Ch4 dc bus 2 load current I_{d2} (10 A/div). Time scale of 30 ms/div.

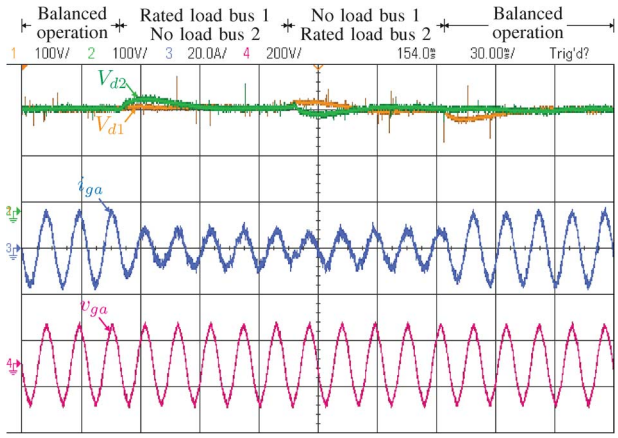

Fig. 16. Experimental results for PEV charging station prototype, VOC signals. Ch1 dc bus 1 voltage V_{d1} (100 V/div). Ch2 dc bus 2 voltage V_{d2} (100 V/div). Ch3 input current i_{ga} (20 A/div). Ch4 grid voltage v_{ga}(200 V/div). Time scale of 30 ms/div.

A. Dynamic Response

The dynamic performance of the charging station is presented in Figs. 15 and 16. It can be seen that the overall behavior of the system is very close to the simulation results.

The dc currents are presented in Fig. 15. The control algorithm is able to extend the balanced operation of the NPC by adjusting the system currents through the bidirectional boost. As it was shown in the previous section, the boost generates a negative current to compensate the no load condition on the lower bus, and positive for the no load condition on the upper bus. It can be seen that the response of the controller allows reaching steady state within two fundamental cycles. The main difference with the simulation results is the response of the relay as it exhibits a small delay in the disconnection of the loads.

The evolution of the main controlled variables in the VOC loop is presented in Fig. 16; it can be seen that the system is able to maintain the balance on the dc voltages during the whole test, presenting minimal deviations from its reference in the transient periods. It can be seen that, in steady state, the voltages V_{d1} and V_{d2} are perfectly balanced. This balance at the dc side allows to have a high input current quality, as it can be seen in the evolution of i_{ga}. This current is kept highly sinusoidal during the rated load condition, whereas during the unbalanced operation, its quality decreases accordingly with the reduction on the fundamental amplitude. In addition, it can be seen that the system operates with unity power factor during the whole test as the grid current is kept in phase with the grid voltage.

B. Steady-State Analysis

The waveforms for the voltages generated by the converter are presented in Fig. 17, showing both, the phase to neutral v_{az} and the line-to-line v_{ab} during steady-state operation. During the balanced operation, it is clear that no dc bias is been injected to v_{az} as there is no current flowing through the converter neutral point. The waveform presents half-wave symmetry, leading to a harmonic content free of even-order harmonics. The spectrum provided shows that the dominant harmonics are located in the sidebands around the component m_f. The resulting waveform for v_{ab} presents a steeped waveform with five levels, clearly defined due to the proper regulation of the mid-point voltage.

The dc drift injected by the midpoint controller becomes obvious in Fig. 17(b). In Case II, the system is compensating the no load condition in the lower bus by injecting a positive dc value, making the pulses wider in the positive half-cycle. Because of this, the symmetry in the generated voltage is missed, leading to the appearance of even-order components in their spectrums, which will have an impact on the demanded current distortion. Nevertheless, as the compensation is injected equally to the three phases of the converter, the line-to-line voltages present a zero dc value in all the scenarios. It is interesting to note that the dominant harmonics of the current have shifted to lower frequencies, situation which can be explained by the loss of half-wave symmetry.

To complete the analysis in steady state, the ac side quantities are illustrated in Fig. 18. The experimental waveforms for the rated load condition of Case I are presented in Fig. 18(a). The results obtained confirm the correct performance of the proposed control scheme. The accuracy on the control of the

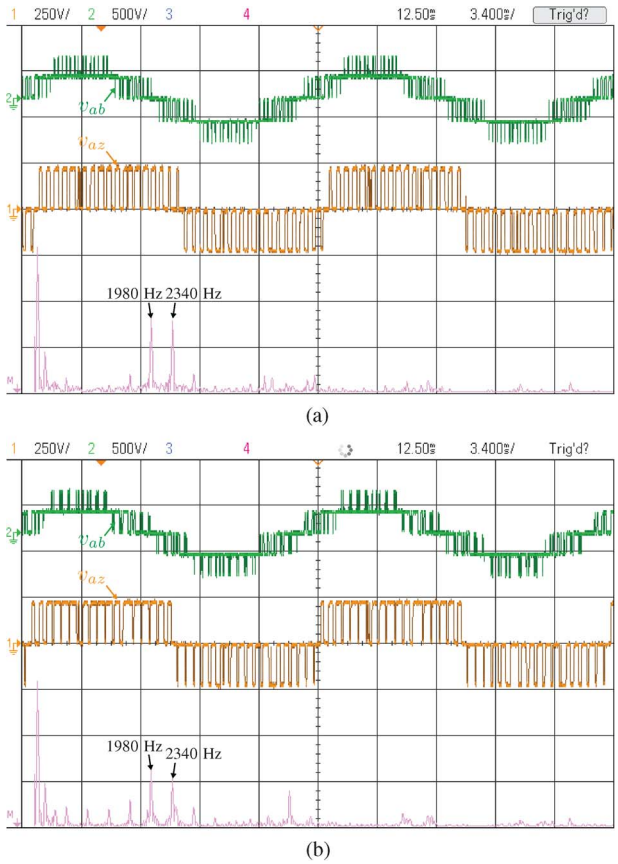

Fig. 17. Steady-state analysis of the converter voltages. Ch1 converter voltage v_{az} (250 V/div). Ch2 line-to-line voltage v_{ab} (500 V/div). ChM FFT for v_{az} (20 V/div, Span 10 kHz, Center 4.8 kHz): (a) Case I, balanced operation. (b) Case II, unbalanced operation in bus 2. Time scale 3.4 ms/div.

midpoint voltage becomes clear as the dc buses voltages are kept balanced, leading to high-quality currents at the input side. The current i_{ga} exhibits a highly sinusoidal behavior, with a fundamental of 15.35 A, reduced ripple, and is in phase with v_{ga}, resulting in a THD of 5.8% for the rated load condition. It also becomes evident the harmonic distortion present in the grid voltage. Then, in the unbalanced operation case of Fig. 18(b), it can be seen that the system is able to operate properly even if one of the loads is disconnected at the dc side. The current is kept sinusoidal, but its ripple has increased; this is explained by the reduction of fundamental component of the current to 7.58 A, and as it was established earlier, the modulation index in grid tied operation with unity power factor varies slightly under different load conditions; therefore, the amplitude of the high frequency components is kept almost constant, increasing its influence on the demanded current. This, along the lack of symmetry in the generated voltage, alters the distribution of the harmonics components, shifting the dominant ones to lower orders. This is confirmed in the input current spectrum shown in Fig. 18(a) and (b), showing that under balance operation, the dominant harmonics of i_{ga} are located in the sidebands around $2m_f$, but in the presence of unbalances, most of the energy is concentrated around m_f, and thus are less mitigated by the action of the input filter.

The grid current THD under unbalances reaches a 14.9%, which corresponds to a total demand distortion (TDD) of

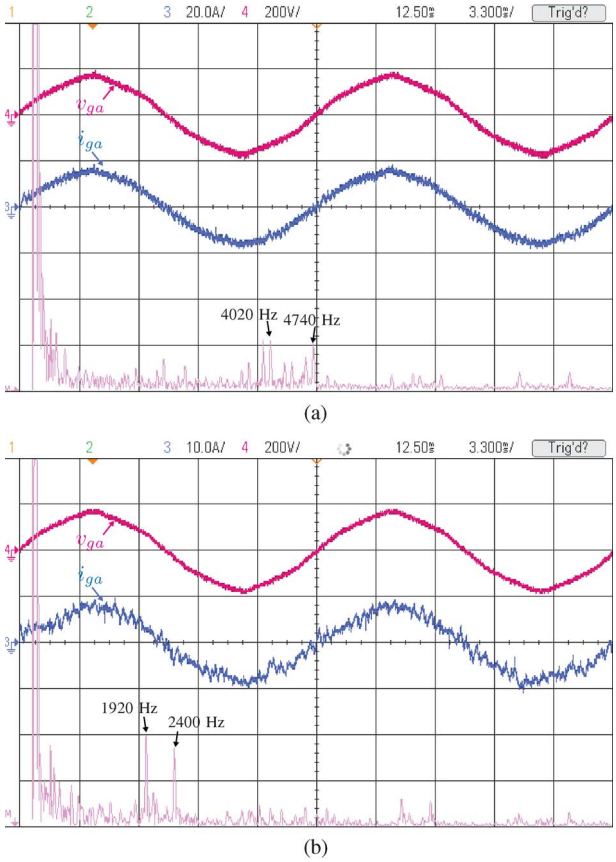

Fig. 18. Steady-state analysis of the input signals. Ch3 input current i_{ga} (20 A/div). Ch4 grid voltage v_{ga} (200 V/div). ChM FFT i_{ga} (100 mA/div, Span 10 kHz, Center 4.8 kHz): (a) Case I, balanced operation. (b) Case II, unbalanced operation in bus 2. Time scale of 3.4 ms/div.

7.35%. This is within the admissible limits of the grid code for the intended power levels $(20 < I_{sc}/I_L < 50)$ [26]. Furthermore, if the unbalanced operation does not exceed one hour in length, it will be considered a unusual condition, and the system will meet the grid code regardless the I_{sc}/I_L ratio.

VI. Conclusion

A novel architecture for fast charging stations for PEVs has been proposed and validated. It is based in the use of a single grid-tied NPC converter, enabling a bipolar dc bus. Its main features are the megawatt range capability, a single ac–dc stage for powering several charging units, the maintenance of the step-down effort of the chargers, balanced operation during any load scenario, and the possibility to include additional storage or generating units into the system. The structure can be installed in different locations within the city, enabling alternatives for refueling the PEVs in shorter times, in order to increase its acceptance.

The use of a multilevel converter also enables the application in MV (lower currents, smaller ac chokes), and improved THD and power quality. In addition, it enables a possible scale up in the power ratings if needed. The limited unbalanced operation of the converter was used to provide a complementary solution and overcome its limits, enabling the operation in any load scenario.

The balancing concept allows to reduce the dc flowing in the balancing circuit, to only a fraction of the demanded current, allowing to reduce the stress on the switches, the size of the inductor and also use higher switching frequencies. This is possible because the scheme exploits the balancing capabilities of the modulator and only uses the balancing circuit as a complement.

The distributed dc bus structure allows to reduce the power conversion stages in the system, reducing the costs and improving the overall efficiency. In addition, it facilitates the integration of PV generation and energy storage systems, allowing the opportunity to reduce the power demand of the chargers and provide support to the grid.

Further research work on the configuration can include: analysis of the possibility to use the fourth leg for fault-tolerant operation; a reliability and availability analysis; efficiency analysis; and a comparison to a nonintegrated modular configuration (one charger per vehicle).

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Sebastian Rivera (S'10) was born in Valparaiso, Chile, in 1986. He received the B.Sc. and M.Sc. degrees in electronics engineering from the Universidad Tecnica Federico Santa Maria, Valparaiso, Chile, in 2007 and 2011, respectively. He is currently working toward the Ph.D. in electrical and computer engineering at the Centre for Urban Energy, Ryerson University, Toronto, ON, Canada.

His research interests include multilevel converters, renewable energy conversion systems, and electric vehicles.

Mr. Rivera received the Emerging Leaders in the Americas Program Scholarship from the Canadian Bureau for International Education in 2010, the Ph.D. Scholarship from the Chilean National Commission for Scientific and Technological Research (CONICYT) in 2011, and the 2013 Graduate Research Excellence Award from Ryerson University.

Bin Wu (S'89–M'92–SM'99–F'08) received the M.A.Sc. and Ph.D. degrees in electrical and computer engineering from the University of Toronto, Toronto, ON, Canada in 1989 and 1993, respectively.

In 1993, he joined Ryerson University, Toronto, where he is currently a Professor and Senior NSERC/Rockwell Automation Industrial Research Chair in Power Electronics and Electric Drives. He has published more than 300 technical papers, authored/coauthored two Wiley-IEEE Press books, and holds more than 25 issued/pending patents in the area of power conversion, medium-voltage drives, and renewable energy systems.

Dr. Wu received the Gold Medal of the Governor General of Canada in 1993, the Premier's Research Excellence Award in 2001, NSERC Synergy Award for Innovation in 2002, Ryerson Distinguished Scholar Award in 2003, and the YSGS Outstanding Contribution to Graduate Education Award and the Professional Engineers Ontario Engineering Excellence Medal in 2014. He is a Fellow of the Engineering Institute of Canada and Canadian Academy of Engineering.

Samir Kouro (S'04–M'08) received the M.Sc. and Ph.D. degrees in electronics engineering from the Universidad Tecnica Federico Santa Maria (UTFSM), Chile, in 2004 and 2008, respectively.

In 2004, he joined the Department of Electronics Engineering, UTFSM, where he currently is a Research Academic. From 2009 to 2011, he was a Postdoctoral Fellow with the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada. He is a coauthor of one book, four book chapters, and over 70 refereed journal and conference papers. His research interests include power electronics, photovoltaic and wind energy conversion systems.

Dr. Kouro served as a Co-Guest Editor for two Special Sections of IEEE TRANSACTIONS. He received the 2008 *IEEE Industrial Electronics Magazine* Best Paper Award, the 2011 IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS Best Paper Award, the 2012 *IEEE Industry Applications Magazine* First Prize Paper Award, and the 2012 IEEE PELS Richard M. Bass Outstanding Young Power Electronics Engineer Award.

Venkata Yaramasu (S'08–M'14) was born in Karumanchi, India. He received the M.E. degree in electrical engineering from Shri Govindram Seksaria Institute of Technology and Science, Indore, India, in 2008 and the Ph.D. degree from Ryerson University, Toronto, ON, Canada, in 2014.

He is currently a Postdoctoral Fellow with Ryerson University. His research interests include renewable energy, high-power converters, electric vehicles, and predictive control.

Dr. Yaramasu received six Best Student Paper Awards and two first prizes in National Level Technical Quiz Competitions during his undergraduate studies in India. During his Ph.D. studies at Ryerson University, he received three first prizes in Poster Competitions, three Student Research Awards from the Toronto Hydro and Connect Canada, three Research Excellence Awards from the Electrical and Computer Engineering Department, and a Best Teaching Assistant Award from the Faculty of Engineering and Architectural Science.

Jiacheng Wang (S'07–M'12) received the B.Sc. and M.A.Sc. degrees from Shanghai Jiao Tong University, Shanghai, China, in 2001 and 2005, respectively, and the Ph.D. degree from Ryerson University, Toronto, ON, Canada, in 2012, all in electrical engineering.

From 2005 to 2006, he was with the Rockwell Automation Shanghai Research Center. From 2011 to 2013, he was a Postdoctoral Fellow with Ryerson University. He is currently an Assistant Professor with the School of Mechatronic Systems Engineering, Simon Fraser University, Surrey, BC, Canada. His main research interests include power conversion and control technologies and their applications in various energy systems.