Predictive Current Control of Grid-Connected Neutral-Point Clamped Converter

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***Abstract*— this paper provides the reader with a detailed description of the Predictive Current Control (PCC) topology for a Three-Level Neutral-Point Clamped (3L-NPC) converter. The process of implementing a real time simulation models is discussed. Also, it illustrates how refining and improving simulation models impact the overall performance of the 3L-NPC converter. The PCC topology is based on first implementing simulation models that cover a definite number of possible switching states for the 3L-NPC converter. A cost function is developed to make the best decision that minimizes the error. Also, it regulates current to follow the reference current. Simulation models are transferred to the converter as gating signals through DS1103. The proposed method is verified by simulation and experimental results. The authors hope that this paper serves as a reference, and base for future improvements in the predictive current control area.**

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I. INTRODUCTION

The grid connected converter (GCC) is a crucial component of modern power conversion systems. GCCs use is becoming more of a necessity due to its flexibility in converting various power applications and its conversion capabilities for different energy resources such as photovoltaic, wind turbines, and motor drives. Nowadays, renewable energy resources is being used more to produce electricity compared to last decade [1]. Recently, different controlling topologies has been developed such as model predictive control (MPC).

Various controlling techniques can be applied on GCCs. Currently, Classical controlling topologies are more common such as Hysteresis Current Control, and Linear Current Control with PWM. The hysteresis current control is common due to its simple implementation where the controlling objectives are the relay band, and the error current [2]. Linear current control uses a proportional integral (PI) to regulate produced voltage according to the reference voltage [3]. Classical topologies can be less effective depending on different aspects such as high frequency, immediate response, and the amount of harmonics produced. Predictive Current Control (PCC) is one of the new emerging controlling topologies in the field. The PCC principle is based on predicting the future behaviour of the converter. PCC predicts the variables for each switching state knowing a finite number of switching states. A cost function model is designed to choose the best switching state option that minimizes the cost function based on the predicted variables. PCC has been proven to be compatible with Neutral Clamped Point (NPC) converters [2].

Multilevel converters are widely used in power applications with power values more than 2-3 MW such as wind turbines [4]. In particular, the three level Neutral Clamped Point (NPC) converter. The three level NPC converter is more efficient and performs better than the standard two level converter. The voltage waveforms produced by the three-level NPC converter is better than the two-level converter. Also, NPC topology reduces the switching losses which makes it more efficient. In addition, the current output ripple is less, and the total supply voltage is split into positive and negative by switching only one half of the voltage which also reduce the switching loss due to cutting it by half [5].

The three-level NPC converters are widely used in high power applications particularly Megawatt level. A lot of research has been conducted regarding the 2-level NPC converters, and the MPC topologies. Nevertheless, authors contribution is aiming for education purposes. Improvements, and new contribution to PCC and 3-L NPC converter is barely discussed [6]. A small improvement in the PCC models could make a crucial impact on the overall performance of the converter. A little improvement in the converter's efficiency could save millions of dollars due to the fact that these type of converters work on high power applications. This paper provides improved controlling schemes in terms of PCC. The improved simulation models increases the efficiency of the 3-L NPC converter by approximately 1-2% by reducing the total amount of harmonics produced. The proposed technique has been verified through tests and experiments. The team has built a 3-L NPC converter, and implemented improved PCC models using MATLAB/Simulink. Simulation models were transferred to dSPACE DS1103-based rapid prototyping and real-time implementation. The implemented PCC models were effective and increased the efficiency of the converter.

This paper is organized as follows: Section II discusses the PCC strategy. Simulink implementation of PCC scheme is given in Section III. Section IV contains the PCC strategy. The simulation and experimental results are outlined in Section V, and finally conclusions are discussed in Section VI.

II. PCC STRATEGY

The PCC algorithm is based on the model of the system. From this model, it is possible to predict the behavior of the system according to every possible switching state of the inverter. It implements the stationary (αβ) frame which involves less burden of computation. By using the neutral point clamped (NPC) converter, the function of this model can be achieved.

A. The modeling of the NPC converter

The NPC converter is the most widely used in all types of industrial applications [7], [8]. The technology of high-voltage insulated-gate bipolar transistors (IGBTs) is applied for the NPC converter. The clamping diode is used to connect the neutral point N to the midpoint of the IGBTs and this neutral point *N* generates an additional voltage level. The NPC features IGBTs and is more suitable for back-to-back (BTB) regenerative applications. The NPC has a simpler circuit structure, which leads to a smaller footprint. As a result, the NPC inverter can significantly increase efficiency. The modeling of the NPC converter is shown in Figure 2.1

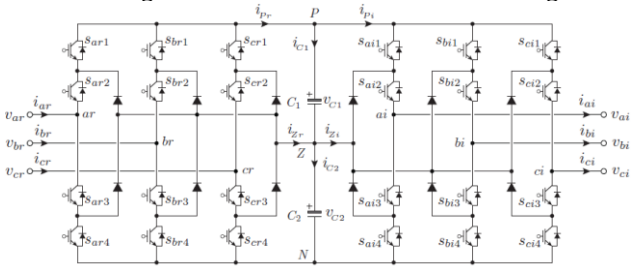


Figure 2.1 Power circuit of BTB connected NPC converter.

DC branch currents are obtained below with the help of switching vectors:

$$\begin{bmatrix} i_p \\ i_z \\ i_n \end{bmatrix} = \begin{bmatrix} \mathbf{S_a}[2] & \mathbf{S_b}[2] & \mathbf{S_c}[2] \\ \mathbf{S_a}[2] & \mathbf{S_b}[2] & \mathbf{S_c}[2] \\ \mathbf{S_a}[2] & \mathbf{S_b}[2] & \mathbf{S_c}[2] \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (1)$$

Output voltages and input DC branch currents for all possible switching states are provided in Table I.

Table 1

Switching Vector	Switching Signals				Output Voltage	Input Currents		
S_x	s_{x1}	s_{x2}	s_{x3}	s_{x4}	v_{xN}	i_P	i_Z	i_N
[2]	'1'	'1'	'0'	'0'	$v_{C1} + v_{C2}$	i_x	0	0
[1]	'0'	'1'	'1'	'0'	v_{C2}	0	i_x	0
[0]	'0'	'0'	'1'	'1'	0	0	0	i_x

B. Stationary Switching States

For a three-phase balanced NPC converter with three modes in each phase, there are $3^3 = 27$ different possible ways (switching states) to connect the output terminals to DC-link and neutral points. As a result, 19 different voltage vectors (V_0 to V_{18}) are used to achieve these 27 different states. The space vector diagram for the NPC converter is shown in Figure 2.1.

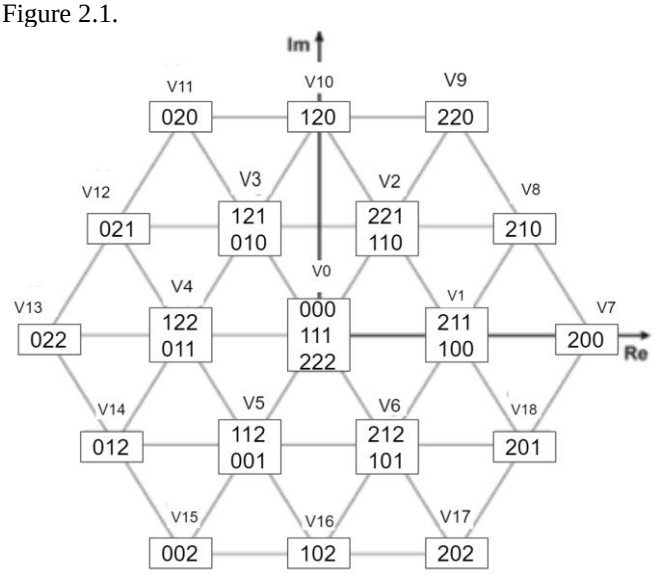


Figure 2.2 Possible voltage vectors and switching states for NPC converter

Using the abc/αβ transformation, the αβ-frame grid voltages are estimated from the natural (abc) frame grid voltages are obtained as follows:

$$\begin{bmatrix} v_{\alpha g} \\ v_{\beta g} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} \quad (2)$$

Where, v_{ag}, v_{bg}, and v_{cg} are the three-phase grid voltages; $v_{\alpha g}$ and $v_{\beta g}$ are the stationary frame grid voltages.

In order to get DC current gains, it is necessary to convert the possible voltage vectors to upper-Leg switching signals. Then, we can obtain DC current gains by using table 2.

Table 2: SWITCHING STATES AND DC CURRENT GAINS

Switching vector		DC Current Gains	
s_{x1}	s_{x2}	k_{x1}	k_{x2}
1	1	-1	-1
0	1	-1	0
0	0	0	0

The complete PCC block diagram in α β -frame for a grid-connected NPC converter is shown in Fig. 2.3. The control system performs the following functions: grid active power control through the d-axis current control, grid reactive power control through the q-axis current control, and grid synchronization.

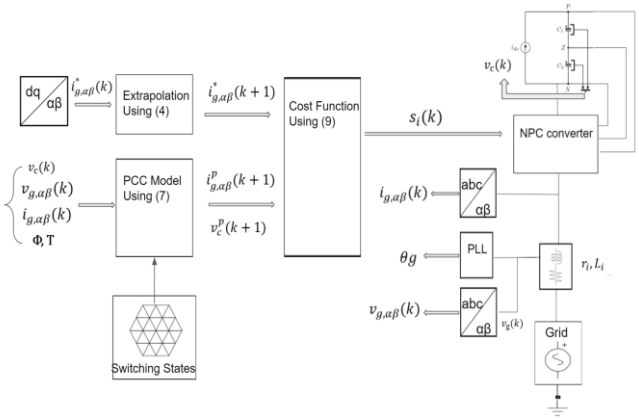


Figure 2.3 Block diagram of PCC scheme for grid-connected NPC converter

B. Design Procedure

1. Estimation of Grid Voltage Angle

To perform grid synchronization, the grid voltage angle θ_g is estimated from the measured three-phase grid voltages. It is obtained by the phase-locked loop (PLL) as shown below [9]:

$$\theta g = \tan^{-1}\left(\frac{v_{\beta g}}{v_{\alpha g}}\right) \quad (3)$$

2. Calculation of Reference Grid Currents

With the help of θ_g, the *dq*-frame reference grid currents into the α β -frame as shown below:

$$\begin{bmatrix} i^*_{\alpha g}(k) \\ i^*_{\beta g}(k) \end{bmatrix} = \begin{bmatrix} \cos\theta g(k) & -\sin\theta g(k) \\ sin\,\theta g(k) & cos\,\theta g(k) \end{bmatrix} \begin{bmatrix} i^*_{dg}(k) \\ i^*_{qg}(k) \end{bmatrix} \quad (4)$$

3. Extrapolation of Reference Grid Currents

To compute the grid current error at (k+2) sampling instant, the α β -axis reference grid currents are extrapolated to (k + 2) state with the help of second-order Lagrange extrapolation as follows [10]:

$$i^*_{\alpha g}(\mathrm{k}+2) = 6i^*_{\alpha g}(\mathrm{k}) - 8i^*_{\alpha g}(\mathrm{k}-1) + 3i^*_{\alpha g}(\mathrm{k}-2)$$
$$i^*_{\beta g}(\mathrm{k}+2) = 6i^*_{\beta g}(\mathrm{k}) - 8i^*_{\beta g}(\mathrm{k}-1) + 3i^*_{\beta g}(\mathrm{k}-2) \quad (5)$$

4. Prediction of Future Grid Currents

The continuous-time grid current dynamic model in α β -frame is presented below [11]:

$$\frac{d}{dt}\begin{bmatrix} v_{\alpha g} \\ v_{\beta g} \end{bmatrix} = \mathbf{M}\begin{bmatrix} v_{\alpha g} \\ v_{\beta g} \end{bmatrix} + \mathbf{N}\begin{bmatrix} v_{\alpha g} \\ v_{\beta g} \end{bmatrix} - \mathbf{N}\begin{bmatrix} v_{\alpha g} \\ v_{\beta g} \end{bmatrix} \quad (6)$$

Where continuous-time parameters **M** and **N** are defined by,

$$\mathbf{M} = \begin{bmatrix} -\frac{r_i}{L_i} & 0 \\ 0 & -\frac{r_i}{L_i} \end{bmatrix}, \quad \mathbf{N} = \begin{bmatrix} \frac{1}{L_i} & 0 \\ 0 & \frac{1}{L_i} \end{bmatrix} \quad (7)$$

The discrete-time model on αβ frame of grid currents at (k+1) state is expressed as follows

$$\begin{bmatrix} i^p_{\alpha g}(k+1) \\ i^p_{\beta g}(k+1) \end{bmatrix} = \mathbf{\Phi}\begin{bmatrix} i_{\alpha g}(k) \\ i_{\beta g}(k) \end{bmatrix} + \mathbf{T_i}\begin{bmatrix} v^p_{\alpha i}(k) \\ v^p_{\beta i}(k) \end{bmatrix} + \mathbf{T_g}\begin{bmatrix} v_{\alpha g}(k) \\ v_{\beta g}(k) \end{bmatrix} \quad (8)$$

Where the superscript *p* refers to the predicted variable; **Φ**, $\mathbf{T_i}$, $\mathbf{T_g}$ are defined as follow:

$$\mathbf{\Phi} = \mathbf{I} + \boldsymbol{A}\,\boldsymbol{T_s},$$

$$\mathbf{T_i} = \begin{bmatrix} \frac{T_s}{L_i} & \mathbf{0} \\ \mathbf{0} & \frac{T_s}{L_i} \end{bmatrix} \qquad \mathbf{T_g} = \begin{bmatrix} -\frac{T_s}{L_i} & \mathbf{0} \\ \mathbf{0} & -\frac{T_s}{L_i} \end{bmatrix} \quad (9)$$

Where **I** is second-order unitary matrix.

5. Cost Function Minimization

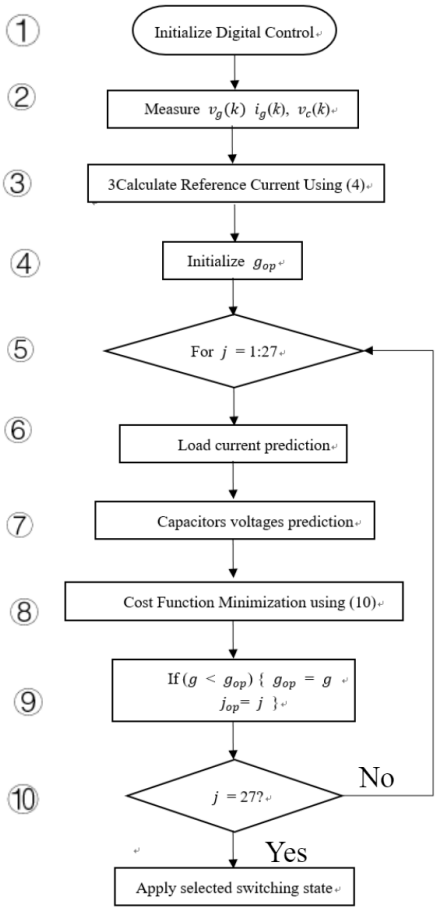
Using the offline computed discrete-time parameters, the future grid currents can be predicted. After that, cost function minimization can be obtained as follows:

$$g_i = (i^*_{\alpha g}(k+2) - i^p_{\alpha g}(k+2))^2 + (i^*_{\beta g}(k+2) - i^p_{\beta g}(k+2))^2 + \lambda_{dc,i} * [v^p_{c1}(k+2) - v^p_{c2}(k+2)]^2 \quad (10)$$

Where $i_{\alpha g}$, $i_{\beta g}$ are the stationary currents V_{c1}, V_{c2} are the DC-link capacitors voltages. $\lambda_{dc,i}$ is weighting factor for DC-link capacitors voltage.

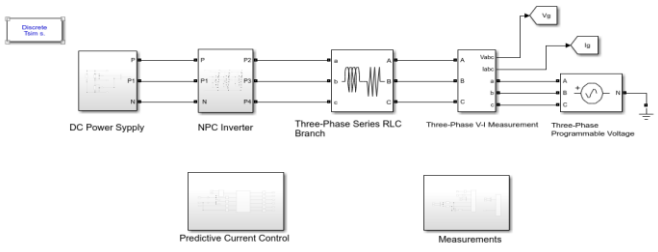
C. Control Algorithm

The flowchart of the PCC algorithm for grid-connected NPC inverter is presented in Figure 3.4. The Feedback Signals are measured in block 2. The reference gird currents $i_{\alpha\beta}$ is calculated in block 3. Initial value for cost function is defined in block 4. Then, the strategy enters a loop between blocks 5, 10. The NPC inverter terminal voltage, grid currents, and DC-link capacitors voltage are predicted for 27 times in 6, 7. The cost function is carried out in block 8. In block 9, the optimal vector j_{op} that provides simultaneous control of the grid current and the DC link capacitor voltage is selected. The last block is used to apply the selected switching state.



III. SIMULINK IMPLEMENTATION OF PCC SCHEME

This section describes the MATLAB/Simulink implementation of PCC scheme for grid-connected 2L-VSC. The simulation files are developed by using the Simscape toolbox in MATLAB/Simulink 2017b release software. Table 4 shows the overall system for parameters.



Block diagram of the ab-frame PPC scheme for grid-connected NPC inverter

The GCC_PCC_Init.m script file is to initialization file which contains parameters for the system. The GCC_PCC_Init.m script file shown table 4 contains model parameters.

```
1 -    clc, clear all, close all
2 -     Ts = 20e-6;
3 -     Tsim = 2e-6;
4 -     Sg = 5000;
5 -     Vgll = 208;
6 -     Ig = 13.88;
7 -     Fg = 60;
8 -     ri = 0.1348;
9 -     Li = 5.65e-3;
10 -    Cl = 1000e-6;
11 -    C2 = 1000e-6;
12 -    Vdcr = 367;
13 -    Rdc = 1e-3;
```

The lib parameters.h file contains the parameter values required for the S-function builder.

```
1   //The discrete-time parameters
2   #define P11 0.999522238058405
3   #define P22 0.999522238058405
4   #define Gi11 0.003538977345145
5   #define Gi22 0.003538977345145
6   #define Gg11 -0.003538977345145
7   #define Gg22 -0.003538977345145
```

The lib vectors.h file shown below is required for the S-function builder. The lines 5 and 6 of the code correspond to initial values. The lines of 7 and 8 defines the initial values. The lines of 9 to 11 is to the cost functions value. The lines of 13 to 16 are the vector for output value and predicted DC-link capacitors currents. The structure type for abc is defined in lines 18 to 25. The switching state combinations increase from 8 to 27.

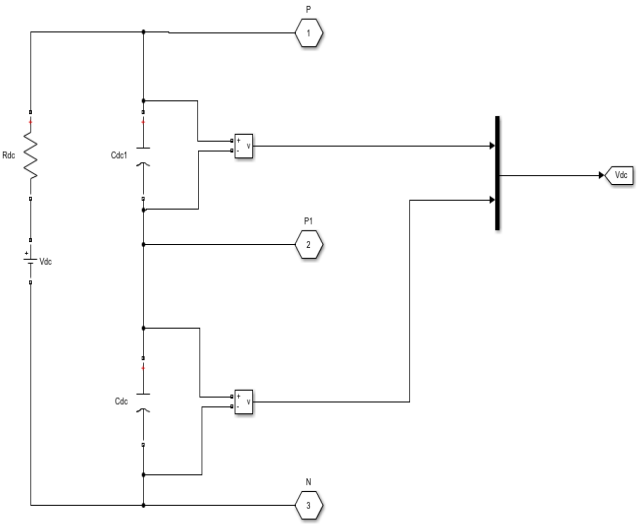


Figure 3.1: DC Power Supply

```
 #define Lambda_dci 0.1089
#define Ts 20e-6
#define C1 1000e-6
#define C2 1000e-6
int j = 0;
 int j_op = 0;
 double g_i = 0.0;
 double g_op = 0.0;
 double g_ial = 0.0;
 double g_ibe = 0.0;
 double g_dc = 0.0;

 double vi_ab[2] = {0.0,0.0};
 double ig_ab_k1[2] = {0.0,0.0};
 double ic_k1[2] = {0.0,0.0};
 double vc_k1[2] = {0.0,0.0};

  typedef struct
 {
    double sabc[3];
    unsigned short int s_i[6];
    double s_i_ab[4];
    double K_i1[3];
    double K_i2[3];
 }
 vector;
 vector vinv[27]=
```

The complete simulation model of -frame PPC scheme for grid -connected NPC inverter is shown in Fig 3.1. And is implemented by the NPC_Grid.slx file. A series of subsystems and blocks consists of overall simulink model: DC power supply, NPC Inverter,three-phase grid,grid voltage, current sensors ,PCC scheme, and measurements. The DC power supply scheme is shown in Fig. 1. The Rdcis the resistance of wire connects the DC power supply. The Cdcis the DC-link capacitor connects the DC power supply as well. The three-phase series RLC branch is to implemented Rdc,Cdcwith capacitance variable. Three-phase series RLC branch is used to implementation branch type by *RL*. The Resistance is set to *ri* and Inductance is set to *Li*. Three -phase V-I measurement is to measure with grid voltages and current sensors. The voltage measurement is set to phase-to-ground. The three-phase programmable voltage source block with positive sequence amplitude Vgll, phase is set to 0 and frequency is set to Fg

```
 {
 0, 0, 0,
 0, 0, 0, 0, 0, 0,
 0, 0, 0, 0,
 0, 0, 0,
 0, 0, 0,

 1, 0, 0,
 0, 1, 0, 0, 0, 0,
 0, 6.666667e-01, 0, 0,
 0, 0, 0,
 -1, 0, 0,

 1, 0, 1,
 0, 1, 0, 0, 0, 1,
 0, 3.333333e-01, 0, -5.773503e-01,
 0, 0, 0,
 -1, 0, -1,

 0, 0, 1,
 0, 0, 0, 0, 0, 1,
 0, -3.333333e-01, 0, -5.773503e-01,
 0, 0, 0,
 0, 0, -1,

 0, 1, 1,
 0, 0, 0, 1, 0, 1,
 0, -6.666667e-01, 0, 0,
 0, 0, 0,
 0, -1, -1,
```

In the data properties tab, all of the input and output of the system are defined with 1-D dimension. The inputs ports are defined as ig_ab_ (2 Rows), vg_ab (2 Rows), ig_ref_k1 (2 Rows), vc (2 Row), ig_abc (3 Rows).The output ports are defined as s_ai1 (1 Row), s_ai2 (1 Row), s_bi1 (1 Row), s_bi2 (1 Row), s_ci1 (1 Row), s_ci2 (1 Row). There are has three includes sections, #include<math.h>, #include “lib_vectors .h”, #include “lib_parameters.h” are add.

```
//P11 =P22 = 1-(ri*Ts/Li); Gi11 = Gi22 = TS/Li; Gg11 = Gg22 = -Ts/Li;
j_op = 1000;
g_op = 1000000000;
for( j = 0; j< 27; j++ )
{
    vi_ab[0] = vc[0] * vinv[j].s_i_ab[0] + vc[1] * vinv[j].s_i_ab[1];
    vi_ab[1] = vc[0] * vinv[j].s_i_ab[2] + vc[1] * vinv[j].s_i_ab[3];
    ig_ab_k1[0] = P11 * ig_ab[0] + Gi11 * vi_ab[0] + Gg11 * vg_ab[0];
    ig_ab_k1[1] = P22 * ig_ab[1] + Gi22 * vi_ab[1] + Gg22 * vg_ab[1];
    ic_k1[0] = vinv[j].K_i1[0]*ig_abc[0] + vinv[j].K_i1[1] * ig_abc[1]
               + vinv[j].K_i1[2] * ig_abc[2];
    ic_k1[1] = vinv[j].K_i2[0] * ig_abc[0] + vinv[j].K_i2[1] * ig_abc[1]
               + vinv[j].K_i2[2]*ig_abc[2];
    vc_k1[0] = vc[0] + (Ts/C1) * ic_k1[0];
    vc_k1[1] = vc[1] + (Ts/C2) * ic_k1[1];
    g_ial = (ig_ref_k1[0] - ig_ab_k1[0]) * (ig_ref_k1[0] - ig_ab_k1[0]);
    g_ibe = (ig_ref_k1[1] - ig_ab_k1[1]) * (ig_ref_k1[1] - ig_ab_k1[1]);
    g_dc = (vc_k1[0] - vc_k1[1]) * (vc_k1[0] - vc_k1[1]);
    g_i = g_ial + g_ibe + Lambda_dci * g_dc;
    if(g_i < g_op)
    {
        j_op = j;
        g_op = g_i;
    }
}
s_ai1[0] = vinv[j_op].s_i[0];
s_ai2[0] = vinv[j_op].s_i[1];
s_bi1[0] = vinv[j_op].s_i[2];
s_bi2[0] = vinv[j_op].s_i[3];
s_ci1[0] = vinv[j_op].s_i[4];
s_ci2[0] = vinv[j_op].s_i[5];
```

The for loop is initialized and j_op is correspond to PCC initialization. The output value are predicted in *vi_ab [0]* and *vi_ab[1]*. *g_i* is the cost function and *ji_opt* is the optimal vector. According to *ji_opt* value, the optimal switching state will produced from the code.

IV. REAL-TIME IMPLEMENTATION of PCC SCHEME

We will be dealing with experimental setup of the PCC Scheme and its transformation into real-time models in this section.

A. Experiment Setup

The complete setup of our PCC Scheme is shown in Figure 4.1

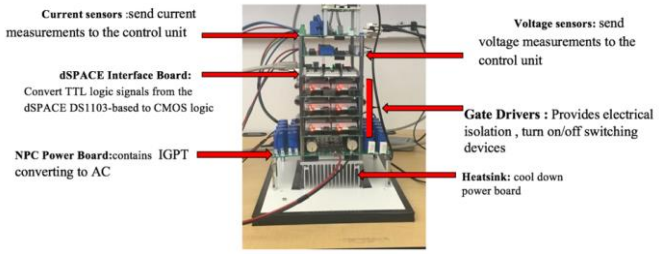


Figure 4.1: Complete PCC Scheme Experimental Setup

An open loop circuit between AC power supplies at 208V (line-to-line, *rms*) and 60 Hz is shown in Figure 4.2 The Magna-Power DC power unit (model number XR50020/208+HS) is powered by AC power and the output DC voltage is connected to the NPC power board. Six Semikron sk 50 mli 066 IGBT modules are used to implement the GCC topology. The Six-phase output terminals of GCC are connected to three harmonic filters 10mH at 20 Amps DC and three resistor TE 2000 B 10R J. The grid phase voltages are measured by the LEM LV25-P sensors. A Dell computer is used to run the dSPACE control desk software and to connect to the DS1103 R&D controller board and CLP1103 connector panel. The gating signals produced by the DS1103 controller are connected to IGBT module gating terminals via 50 pin D-SUB connector, interface board, and Semikron SKHI22B gate drivers.

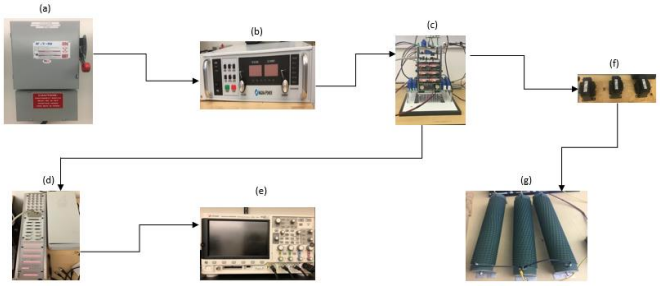


Figure 4.2: Block diagram of experimental setup: (a) three-phase grid, (b)DC power supply, (c) NPC grid converter, (d) DS1103, (e) oscilloscope, (f) harmonic filters, (g) resistor TE 2000 B 10R J.

B. Real-Time Models

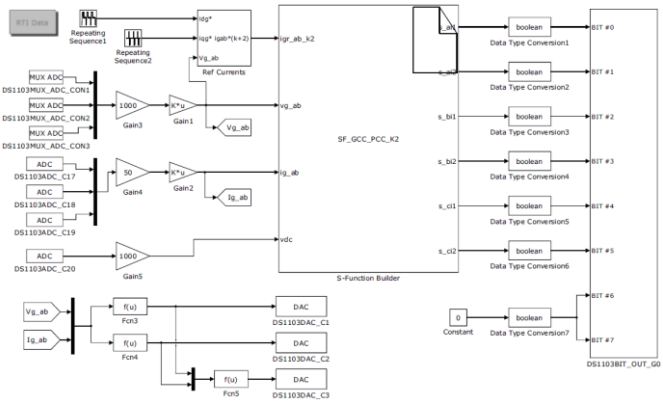


Figure 4.3. Real-time implementation model for PCC scheme [6].

The real-time model for PCC scheme is shown in Figure 4.3. It is implemented by GCC PCC Model in which real time measurements are used instead of simulated measurements. The voltage and current measurements are interfaced to the real-time simulation model via ADC channels of CLP1103 connector panel. The ADC channel gain is 10 and voltage sensors gain is 100; therefore, the three phase grid voltages

(v_{ag}, v_{bg}, v_{cg}) and DC link voltage (v_{dc}) are multiplied by a coefficient of 1000. Similarly, the current sensors gain is 5 and thus the three-phase grid currents (i_{ag}, i_{bg}, i_{cg}) are multiplied by a coefficient of 50. The active, reactive, and apparent powers computed by the DS1103 controller are sent to the Agilent oscilloscopes through CLP1103 DAC channels. The powers are divided by a coefficient of 10,000 to ensure that the inputs to the DAC channels are in ±1 V range. The submodule for predictive current control is shown in Figure 4.4 and for measurement is shown in Figure 4.5

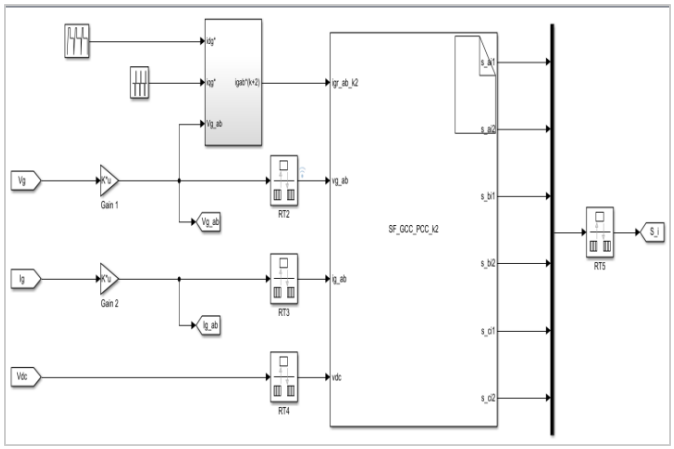


Figure 4.4: Predictive Current Control

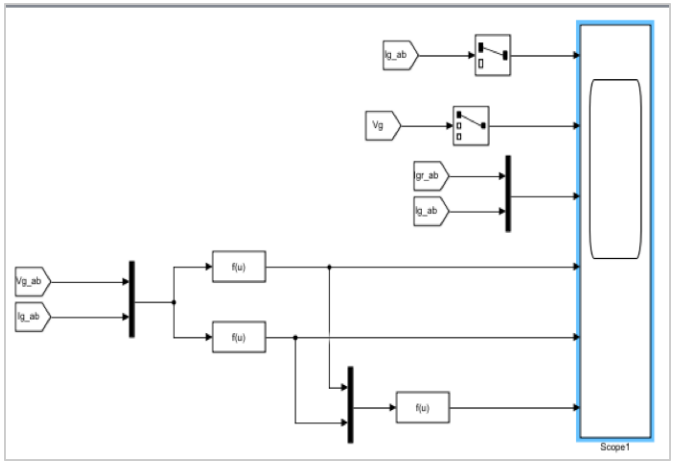


Figure 4.5: Measurement Module

V. RESULTS and ANALYSIS

To validate the proposed design procedure, simulation and experimental tests are conducted using the MATLAB/Simulink software and DS1103 controller, respectively as shown in Figure 5.1 with the parameters as indicated in Table 4.

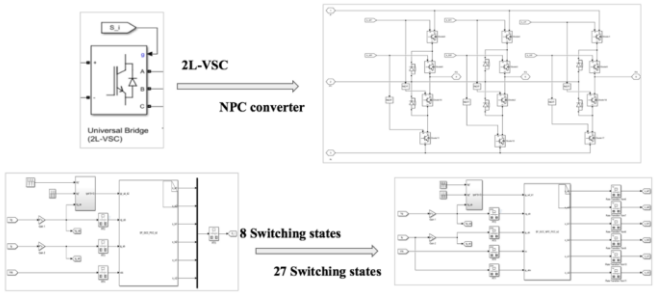


Figure 5.1: PCC for NPC with Grid

Table 4: Rated Parameters for GCC

Parameter	Symbol	Value
Control sampling time	Ts (s)	20 × 10−6
Simulation sampling time	Tsim (s)	2 × 10−6
GCC apparent power	Sg (VA)	5000
Grid phase Voltage	vg (V, *rms*)	208
Grid line current	ig (A, *rms*)	13.88
Grid frequency	fg (Hz)	60
Filter resistance	ri (Ω)	0.1348 (0.02 pu)
Filter inductance	Li (H)	5.65 × 10−3 (0.25 pu)
DC link capacitance	Cdc (F)	1000 × 10−6 (3.26 pu)
Reference DC link voltage	vd∗c (V)	367 (3.062 pu)
DC link resistance	Rdc (Ω)	1 × 10−3 (0.00015 pu)

A. Simulation Results and Analysis

The simulation results with programmed *dq*-axis reference currents are shown in Fig. 5.2 The *d*-axis reference current ($i*_{dg}$) is programmed to increase linearly from 0 pu to 1.0 pu from t = 0 s to 0.4 s. A step change in $i*_{dg}$ from 1.0 pu 0.6 pu is applied at t = 0.8 s. The reference tracking capability of PCC scheme is demonstrated in Figure 5.2 and Figure 5.3

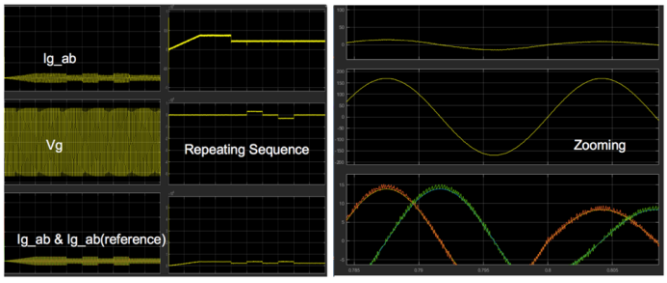


Figure 5.2: Grid Connected 2L-VSC with PCC

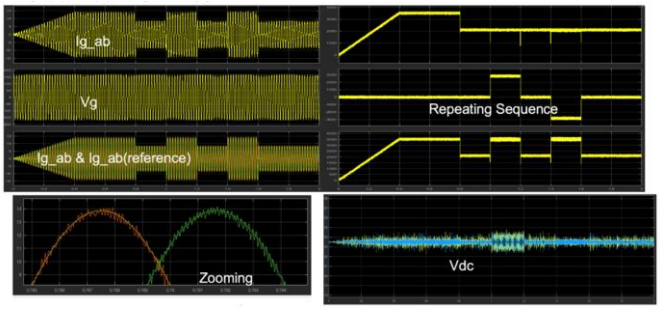


Figure 5.3: Grid Connected NPC with PCC

B. Experimental Results and Analysis

The parameters of the experimental setup are same as the simulation test discussed earlier. The experimental tests are conducted using the similar operating conditions of simulation tests. The experimental results with programmed $i*_{dg}$ and $i*_{qg}$ values. The active and reactive powers follow $i*_{dg}$ and $i*_{qg}$ trajectories similar to the simulation results. Similarly, i_{ag} follows the S_g trajectory. The simulation and experimental results are identical in terms of dynamic response, decoupled control, and steady-state performance show in Figure 5.4 and 5.5

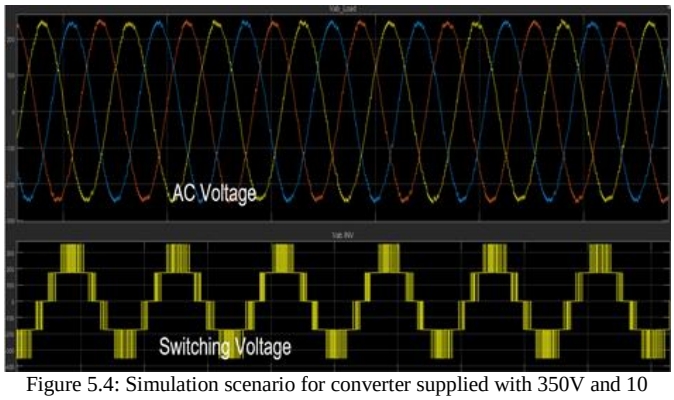


Figure 5.4: Simulation scenario for converter supplied with 350V and 10 Amp DC power, three phase AC waveforms, and five level line to line AC waveform.

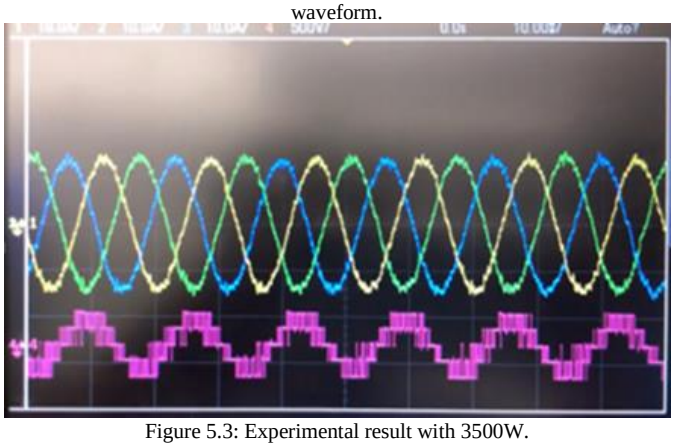


Figure 5.3: Experimental result with 3500W.

VI. CONCLUSIONS

In a world full of technology, power conversion systems plays a major role in maximizing benefits from renewable energy sources. Improving power conversion controlling topologies is important as it is important to build and improve converters. Therefore, this paper focuses on PCC topology, and it provides a detailed description of techniques on improving it. This is based on implementing and improving real-time simulation models that predicts the future behavior of the converter, and make the best decision. This improves the overall performance of the converter, and increases its efficiency based on reducing harmonic distortion through refined simulation models. The paper includes results and analysis illustrating the effectiveness of PCC topology in the overall performance of the 3-L NPC converter. The authors hope that this research would help researchers in the predictive current control area, and serves as a base for future improvements.

APPENDIX

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