1 PURPOSE

The following document defines the requirements for the NAU Capstone project for development of a digital receiver using an FPGA. The final use of digital receiver is to serve as digital demodulator for a communication radio product. The main focus of the project is to develop topology and working VHDL code to meet the specifications listed in the document.

2 PROJECT DESCRIPTION

Receivers are important devices in our society being the major component of such products as cell phones, televisions, etc. Historically receivers have been constructed entirely of analog devices but with advances in digital technology, large portions of receivers are now accomplished using DSP technology.

This project focuses on the DSP portion of the receiver as shown in Figure 21 below, which consists of the ADC, the demodulation function, and the DAC as shown in red. The goal is to digitize the band limited signal provided by an external receiver IF chain, additionally filter the signal as required, demodulate the signal with the selected modulation, audio filter as required, and output the audio signal.

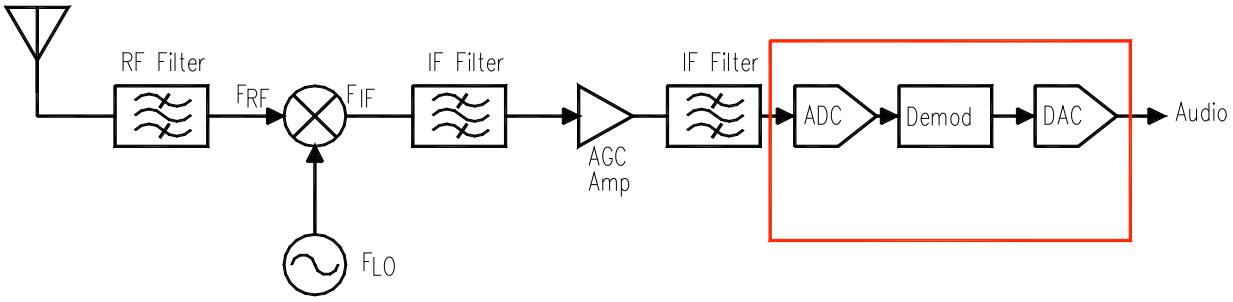

Figure 21: A typical digital receiver.

The demodulation is to be done with an FPGA device since many of the requirements would overload the processing capability of a conventional DSP processor. The FPGA must be interfaced to the analog world through an ADC and the processed signal outputted via a DAC. The receiver design located before the ADC provides band limiting to the ADC but the bandwidth of this filter is wider then the desired information bandwidth to allow selection of multiple receiver bandwidths as required by the communication system. Two bandwidth filters are required by the system of 25 kHz and 8.33 kHz and should be capable of dynamically switching between the filters without reloading the FPGA by grounding an external pin.

Items that are important in a communication system are listed below and these items must be considered in the design and taken into consideration.

Dynamic Ranged:

The input to the receiver will change in amplitude dynamically and must be adjusted to stay within the dynamic ranged of the ADC. The range of signal may be expected to vary by 100 dB. The FPGA must account for >40 dB internally with a constant audio output. Additional AGC would be external to the FGPA and output shall be planned provided to an external AGC amplifier for the additional 60 dB of range. The design does not necessarily need to be demonstrated with the external AGC.

Adjacent channel rejection:

Normal communication channels contain multiple channels of communication and the receiver must reject unwanted channels. Since this is a multiple bandwidth receiver, the adjacent channel filtering will be done in the FPGA using a digital filter. This filter is normally defined by two requirements, the required communication channel bandwidth, and the adjacent channel rejection. The adjacent channel rejection shall be greater than 60 dB.

ADC Dynamic range:

The dynamic range of the ADC is typically limited by noise floor and spurious responses. Consideration should be given to extending the dynamic range by over sampling as much as possible.

The type of modulation chosen for the system can be either FM, AM, or digital modulation but the modulation type should be chosen such that signal generators available at NAU can be used as the signal source.

Specifications:

Input channel frequency, i.e., IF frequency: 75 MHz.

External receiver IF bandwidth: 200 kHz

DSP filter requirements:

25 kHz channels:	-6 dB maximum @ ±10 kHz -40 dB minimum @ ± 17 kHz -60 dB minimum @ ± 22 kHz
and	
8.33 kHz channels:	-6 dB maximum ±2.78 kHz -60 dB minimum ± 7.37 kHz

Audio leveling: The output should include automatic level control for <3 dB audio output variation over the specified input dynamic range

Dynamic range: 100 dB of which 40 dB is to be accomplished in the FPGA

Coding: FPGA coding may be either in Verilog or VHDL. Verilog is preferred.

Modulation: FM and/or AM or other as selected

Temperature range: -30 to +85 C

An Altera DE2 development board is available for utilization in the project and may be satisfactory for completion of the whole project. Review of the building blocks available on this board should be reviewed against the requirements to determine suitability. An additional digital receiver with complete with on board FPGA is also available and may offer the best development platform.

The difficulty of system requirements should be reviewed and an estimation of the time required for each task should be estimated. Some elements of the design may not be obtainable in the timeframe and resources you have available. Therefore, it may be desirable to fully complete a subset of the projects tasks rather then tackle too much work and fail. These factors should be communicated and agreed upon.

Before coding is started a system model should be constructed and simulated to prove your chosen topology will meet the system parameters. A preliminary design review should be completed at this point with a working project plan.

There are multiple possible methods for completing the project. Since the bulk of the project involves the use of a programmable logic device, testing of multiple topologies and comparison of performance should be possible and is encouraged.

3 Major Project Tasks

Project items will include the following:

3.1 Block Diagram and system design

Careful consideration needs to be taken to consider the performance parameters and what outside influences will have on these parameters. If the design is to be parsed out to individuals, interface specifications must be defined between each block.

4 FPGA selection.

The system design and block diagram must be sufficient to estimate the resources required for selection of the programmable part. A recognized methodology for estimating gate requirements, propagation delays, toggle frequency, etc., shall be used and presented at he preliminary design review.

5 FPGA interface circuit design

To interface to the other components of the PLL, additional circuits will be needed. These circuits are the responsibility of the design team and should be fully simulated.

5.1 Validation testing

The working circuit will need to be tested for compliance to the design specifications. This should include simulated timing analysis and vector test

conditions as well as noise performance verification, etc., in the test bed. Adjustment of the final circuit values may be required to meet design goals.

Target testing shall include:

1. Demodulation of a test signal
2. Dynamic range performance
3. Adjacent channel rejection as measured with an on channel and off channel signals.
4. Noise floor as measured by minimum signal level received.
5. Audio output leveling and measured by signal output variation with various levels of input modulation.
6. Audio filtering of the demodulated signal.

5.2Documentation

Final documentation should include a comparison of the design goals to finished results with a white paper that details your calculations and assumptions, compares expected results to the measured results, and lists possible reasons for variations or failures and possible future improvements.

6 TEST CONDITIONS

All specifications pertain to the following input and environmental conditions unless otherwise specified.

6.1Environmental conditions

Temperature range: -55 to +70 C

6.2Alignment procedure

The design should not require alignment except for setting of the reference frequency.